Investigation on Smart Bi-Directional Inverter with Quantitative Reactive Power Compensation and Interleaved DC/DC Converter for Micro-Grid System

by

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All Glory be to God the Father Almighty.

Dedicated to my wife, my son and my parents.

Thanks for their support and trust.

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Abstract

The PhD project aims to develop a smart grid-connected inverter (SGCI) for a micro-grid, which can be applied in a built environment such as a community, and associated power electronic DC/DC converters. The micro-grid generally includes distributed renewable power generators and battery storage.

The SGCI is a bi-directional DC/AC inverter for distributed generation with battery storage installed at its DC side. In one aspect, it is expected the DC/AC inverter functions as a controlled inverter that can deliver expected real power to the power grid with quantitative reactive power compensation (RPC). In other words, all the SGCIs in the community microgrid can share the reactive power of the whole community because a SGCI can quantify its active and reactive power output. It is also expected that the inverter can work in both on-grid and off-grid modes. In other words, the DC/AC inverter functions as a controlled rectifier with high quality power factor correction (PFC), which can deliver expected DC power from the AC power grid at unity power factor. With the above features, battery storage on the DC bus of the SGCI can be charged/discharged through a four-phase, interleaved, bi-directional, boost/buck DC/DC converter (IBDBBC) for distributed renewable power system, either wind or solar PV or hybrid wind/solar PV system. The IBDBBC can discharge power from a low voltage battery to a high voltage DC bus as the IBDBBC operates in boost mode, or it can also draw power from the DC bus to charge the battery as the IBDBBC operates in buck mode.

Based on MATLAB/Simulink, a mathematical model was developed for the grid-connected bi-directional DC/AC inverter that operates as a rectifier with PFC and as a grid-connected inverter (GCI) with expected real power output and quantitative RPC.

In a practical application, the sampling of input signal through AD converter usually has some noise due to common-mode interference; simulation results demonstrate that the second order

generalised integrator (SOGI) has great advantages to prevent interference. Therefore, SOGI can be utilised to construct a pair of orthogonal signals in a single-phase system to instantaneously split grid's active and reactive power to achieve RPC for local community loads. The methodology of the constructed the pair of orthogonal signals was also used to generate the required reference current for the DC/AC inverter when which operated as a single-phase rectifier with PFC.

Using three TI C2000 Solar Inverter DSK Boards, a small lab scale distributed power system was developed. In the lab distributed power system, the operating mode of the inverters could be switched between on-grid and off-grid through instruction from the control centre. The lab test outcomes demonstrate that each distributed power system unit worked properly under loss of power grid signal, simulating grid failure.

Abbreviations

AC	Alternating Current
AC/DC	Alternating Current to Direct Current
AD	Analogue to Digital
APLL	Analogue PLL
CCS	Code Composer Studio
CCM	Continuous Conduction Mode
CPU	Control Processor Unit
CSI	Current Source Inverters
DCM	Discontinuous Conduction Mode
DPLL	Digital PLL
DSP	Digital Signal Processor
DC	Direction Current
DC/AC	Direction Current to Alternating Current
DC/DC	Direction Current to Direction Current
DG	Distributed Generators
DSK	Development Starter Kit
ESS	Energy Storage System
EV	Electrical Vehicle
FPWM	Fuzzy PWM
FPU	Floating-Point Unit
GCI	Grid-Connected Inverter
GCIS	Grid-Connected Inverter System
HCC	Hysteresis Current Control
IBDBBC	Interleaved Bi-directional Boost/Buck DC/DC Converter

IDE	Integrated Development Environment
IGBT	Insulated-Gate Bipolar Transistor
IO	Input and Output
JTAG	Joint Test Action Group
MPPT	Maximum Power Point Tracking
PCC	Point Common Coupling
PFC	Power Factor Correction
PHS	Pumped Hydroelectricity Storage
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PLL	Phase-Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Source
RMS	Root Mean Square
RPC	Reactive Power Compensation
RTXD	Real-time Exchange Data
SGCI	Smart Grid-Connected Inverter
SDK	Solar Inverter Development Kit
SFPLL	Synchronous Frame PLL
SHEPWM	Selective Harmonic Elimination PWM
SOGI	Second Order Generalised Integrator
SOGIPLL	Second Order Generalised Integrator PLL
SPLL	Software PLL
SPWM	Sinusoidal PWM
SSDG	Small Scale Distributed Generators

STACOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VAR	Volt Amperes Reactive
VCO	Voltage Controlled Oscillator
VFD	Variable Frequency Drives
VSI	Voltage Source Inverter

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Chapter 1 Introduction

1.1 Motivation

In the past two decades, renewable power generation, such as wind and solar power, have experienced a considerable growth due to the problems the world faces in the dual challenges of fossil fuel depletion and carbon dioxide emissions (Fthenakis, et al., 2009). However the intermittent nature of renewable energy sources (typically wind and solar energy sources) is a major issue for the renewable power industry. DC/AC inverters play a key role in renewable power generation, which interfaces renewable power generators with the grid. However, a conventional GCI injects power from the renewable power generator directly into the grid, which fluctuates with the intermittent and unstable renewable energy sources.

Furthermore, the increase in generation uncertainty created by intermittent sources, such as photovoltaic (PV) cells and wind turbines, presents a challenge to the system stability of large power grids (Eltawil & Zhao, 2010). Renewable energy sources such as solar and wind are intermittent energy resources, especially as wind speeds and cloud movements cannot be accurately forecast in real time. For the solar energy, the maximum solar radiation occurs at around 13:00 hours each day. That means the power output of a solar PV panel theoretically reaches its maximum at this time despite the domestic demand being minimum. Therefore renewable power systems may operate in troughs of power demand, however the GCIs with an MPPT still output power into the grid in accordance with the code of compliance. Therefore, this may cause a voltage rise in the utility grid, which could result in the generation system being forced to be disconnected from the power grid when the voltage of the utility grid reaches its top limit.

Moreover, for a utility grid to operate properly, it is a prerequisite for GCIs to inject power into the grid when power is available. This means the primary issue of a GCI not being able to generate power even under the situation of best weather conditions for generation while the power grid is cut off for a reason either foreseeable (such as scheduled maintenance and power curtailment when power supply does not meet demand in general) or unforeseeable incidence (such as fire, flood). This is especially the case in some areas of the power system which are relatively vulnerable such as in developing countries in Saharan Africa and South-Asian where there are excellent solar energy sources, but unreliable or unavailable electricity grids.

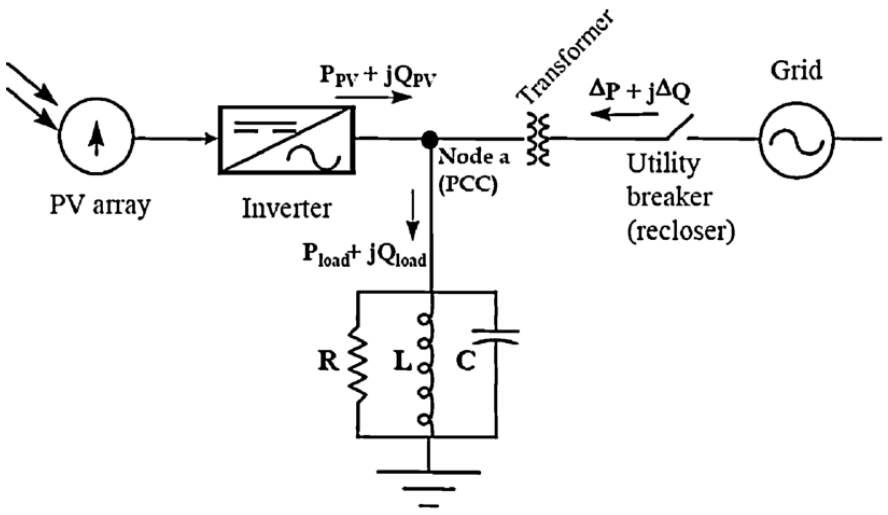


Figure 1- 1 Conventional RPC for solar PV power system

Taken from (Eltawil & Zhao, 2010)

In addition, the increasing application of nonlinear loads, such as induction cookers, large variable frequency drives (VFD), switching-power supplies, induction motors and welding machine, may cause distribution system power quality issues, especially the production of a significant amount of reactive power and harmonics (Renukadevi & Jayanand, 2015). However, conventional distributed generation systems have limited capability to RPC. The use of a complementary external passive parallel RLC (resistor, inductor and capacitor) components or static synchronous compensator (STACOM) at the point common coupling

(PCC) shown in Figure 1-1 can provide compensation (Medina, et al., 2016). This increases the system and operation cost.

Finally, Llaria and Chicco presented that a system based on small-scale cogeneration could be more suitable than a large-scale distributed generation (Llaria, et al., 2011) (Chicco & Mancarella, 2009). Residential roof mounted solar PV system can be considered as a small-scale generation, so each individual small-scale system like that, connected to the same substation or community, can constitute a micro-grid system. But for the residential roof mounted solar PV system or commercial small-scale renewable power system, using Economy 7, a type of electricity tariff based on the time of use, the price of electricity on Economy 7 is very low during night, however night-time is the period of the lowest electricity consumption.

1.2 Aims and objectives

This thesis aims

1) To develop a bi-directional GCI with RPC for a micro-grid by using interconnected small-scale GCIs sharing responsibility for community reactive power.
2) To develop an interleaved bi-directional boost/buck direction current to direction current (DC/DC) converter interfacing the DC link and the battery bank for charging/discharging batteries.

To mitigate the output voltage fluctuation from GCIs and improve customers' profitability, a battery bank at the inverter DC side, is included, interfaced by a bi-directional DC/DC converter with a DC-Bus as shown in Figure 1-2. In the community micro-grid, each individual inverter only injects excess power into the utility grid, generated from the renewable energy source (RES), with the premise that the battery bank is fully charged and the customers' requirements are completely met. During low tariff periods the inverter can be operated as an AC/DC controllable active rectifier to draw power from the utility grid to provide energy to

charge the battery bank by means of the bi-directional boost/buck DC/DC converter. Therefore, the inverter with those two control rules can minimise the end-user's electricity costs.

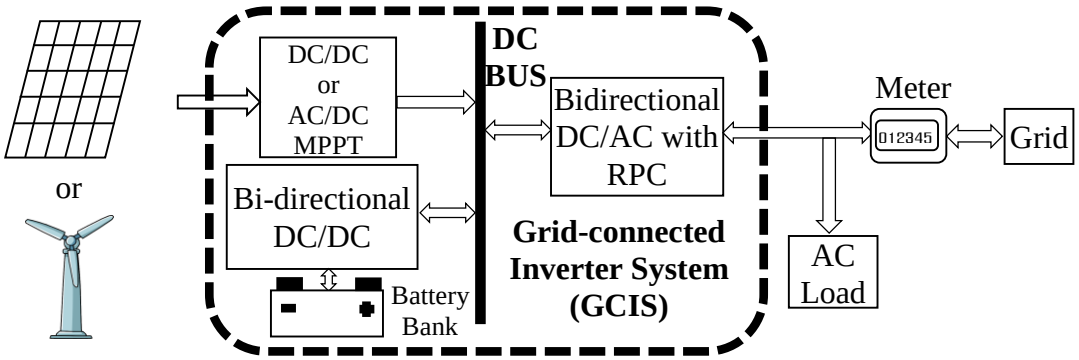


Figure 1- 2 Proposed the diagram of small-scale GCIS

Figure 1-2 presents the community micro-grid formed with a number of individual small-scale GCI system (GCIS), in which, the GCIS is integrated with a maximum power point tracking (MPPT) regulated DC/DC converter connecting solar PV panels or AC/DC converter connecting wind turbine generator, a bi-directional boos-buck DC/DC converters for charging/discharging batteries, and a bi-directional DC/AC inverter with RPC interfacing the DC bus and AC grid. A single GCI cannot provide RPC for a whole system, if each GCIS in the micro-grid system can quantitatively share responsibility RPC for whole system, then the conventional RPC devices or equipment illustrated in Figure 1-1 can be removed at the PCC node.

Figure 1-3 illustrates a diagram of micro-grid system, which consists of solar PV generations, wind turbines, electrical vehicle (EV), public utilities, GCISs and control centre. The Presented GCIS is used to interface between distributed sources and micro-grid.

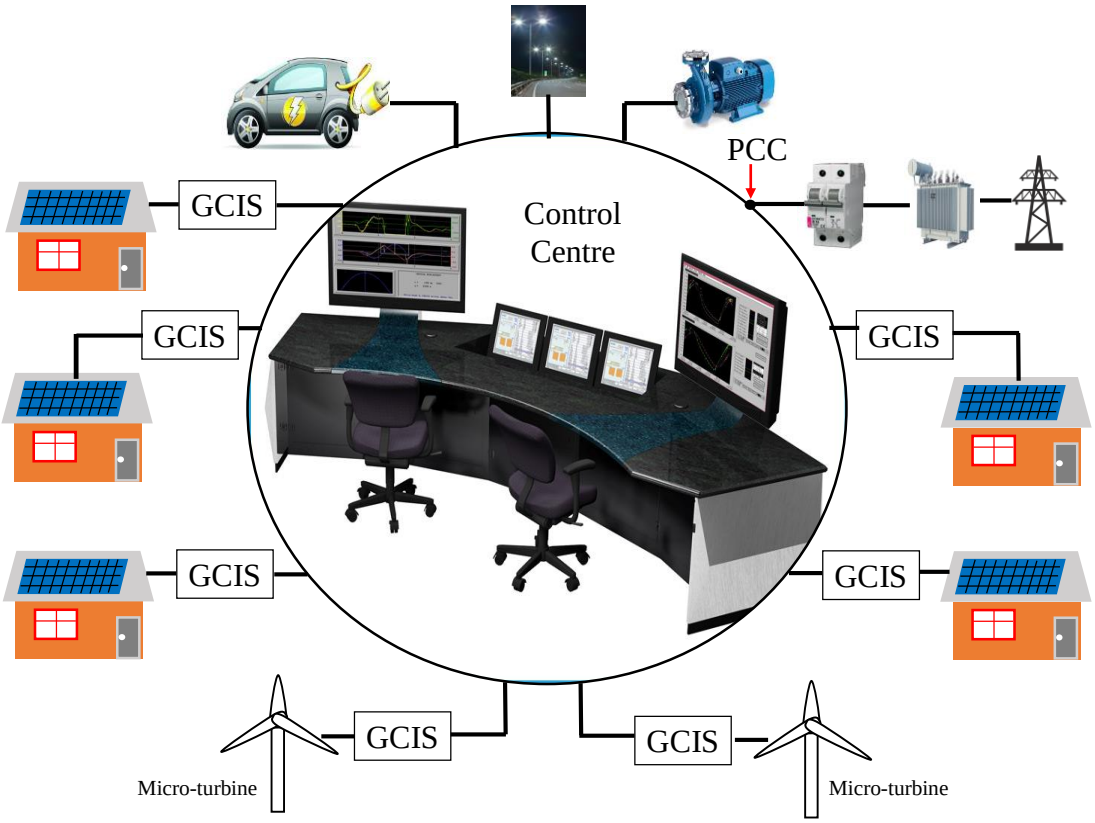


Figure 1- 3 Diagram of smart distributed micro-grid

There are a number of established algorithms that can be employed to implement MPPT for both wind turbines and solar PV systems. Therefore, the MPPT algorithms are not considered in this thesis. To develop a smart GCIS for the micro-grid, the objectives of the project are:

1. To investigate the design process of a phase-locked loop (PLL) based on second order generalised integrator (SOGIPLL) for synchronising with the grid voltage and constructing orthogonal signals.
2. To model a bi-directional multi-phase interleaved boost/buck DC/DC converter.
3. To model an active rectifier with PFC based on the topologies of GCI for single-phase system.
4. To model a controllable active space vector pulse width modulation (SVPWM) rectifier with PFC based on the topologies of GCI for three-phase system.
5. To model a dispatchable single-phase hysteresis band GCI with RPC.

6. To model a dispatchable three-phase SVPWM GCI with RPC.
7. To model multi-inverter sharing RPC for a micro-grid.
8. To compare the results of modelling with measurements on a laboratory system.

1.3 State of the art technologies

Nowadays, with technological developments, many clean renewable energy resources, such as solar, wind, hydro, tidal and biomass power are being utilised without emissions. Although renewable energy resources are clean and favoured by researchers for generation, the high penetration of renewable energy in distributed generation is associated with many new technical challenges in practical applications, such as grid voltage fluctuation, frequency regulation and RPC. Thereby, large amount of GCIs without proper technical infrastructure could have an impact and place significant harmonic stress on the electricity grid (Obi & Bass, 2016), unless the increasing GCIs have the dispatchable characteristics (Zarina, et al., 2012). Hence, during recent years, the micro-grid concept has been introduced, consisting of several alternative sources which can be considered plug-in or –out, while distributing electricity more efficiently and securely (Aghajani, et al., 2015) (Kamankesh, et al., 2016).

A micro-grid is commonly defined as a small community of interconnected loads and small-scale distributed generators (DGs) which can be dispatched or regulated by a control centre. A micro-grid is typically supplied by a MV/LV substation, and generally comprises DG, a smart meter and information communication (Sbordone, et al., 2016). The DG interfaces the resource and the micro-grid, it plays an important role, with the features of maintaining voltage balance, provide peak-shaving, optimise energy flux, and offer auxiliary services, which can be easily plugged-in or -out.

In the future, the numerous unpredictable loads introduced into the micro-grid, such as the expected increase of a number of EV charging stations, could bring chaos to a distributed grid

that has been fluctuating due to the intermittent nature of renewable energy sources. Sbordone et al propose solving these problems (Sbordone, et al., 2016) by the concept of integrating autonomous energy storage system at a location near the substation for reducing variability of power flow, providing balancing support, peak-shaving and load shifting. Panwar et al. present a strategy of incorporating regenerative fuel cells and EVs to solve the problem discussed above (Panwar, et al., 2015). Though the approach of configuring storage devices near a substation could enhance the stability of an entire distributed grid system, for a distributed micro-grid system, except the stabilising the grid, and minimising the user's costs which is also an important factor to be considered.

The voltage source inverter (VSI) is the most widely employed topology for this role with some common filter circuits, *L* (inductor) or *LCL* (inductor, capacitor and inductor), to achieve a DC/AC GCI for distributed generation (Sampaio, et al., 2016). Several related papers present various current control algorithms to feed active power into the grid. In order to enhance the stability of the grid system, the requirement of RPC has drawn more interest from researchers in the past few years.

1.3.1 Techniques related to RPC

The most common volt amperes reactive (VAR) control approach for both small-scale and large-scale distributed generation is ensuring the inverter operates at a constant, unity power factor. The approach of utilising large passive capacitive banks or STACOM, at the PCC node, to maintain unity power factor is widely used. However, the major drawback of these approaches is not being able to inject RPC back to the grid. In other words, these approaches do not offer RPC for domestic loads. Variable power factor is a popular method, in which an inverse relationship between $\frac{\Delta P}{\Delta Q}$ and the ratio of $\frac{R}{X}$ at the PCC is established by setting the voltage variation difference to 0 (Smith, et al., 2011). This method observes the voltage

changes at the PCC to determine the extent of RPC. This is rather similar to the droop control technique, in which active power changing affects the grid frequency and reactive power influences grid voltage magnitude (Samadi, et al., 2014) (Rouzbehi, et al., 2014).

Sampaio et al. present, according to active and reactive power transfer, a strategy to control the power transfer angle by means of stabilising active power output and to control reactive power by reducing voltage magnitude fluctuation, which is actually quite similar to the droop control (Sampaio, et al., 2016).

Liu et al. proposed a topology of a single-stage for a single-phase GCI with wide range RPC, in which 3 full-bridge inverters are connected in series. One of the inverters injects active power into the main grid, and the other two auxiliary inverters interface dedicated energy storage for the grid, providing RPC, see Figure 1-4 (Liu, et al., 2010).

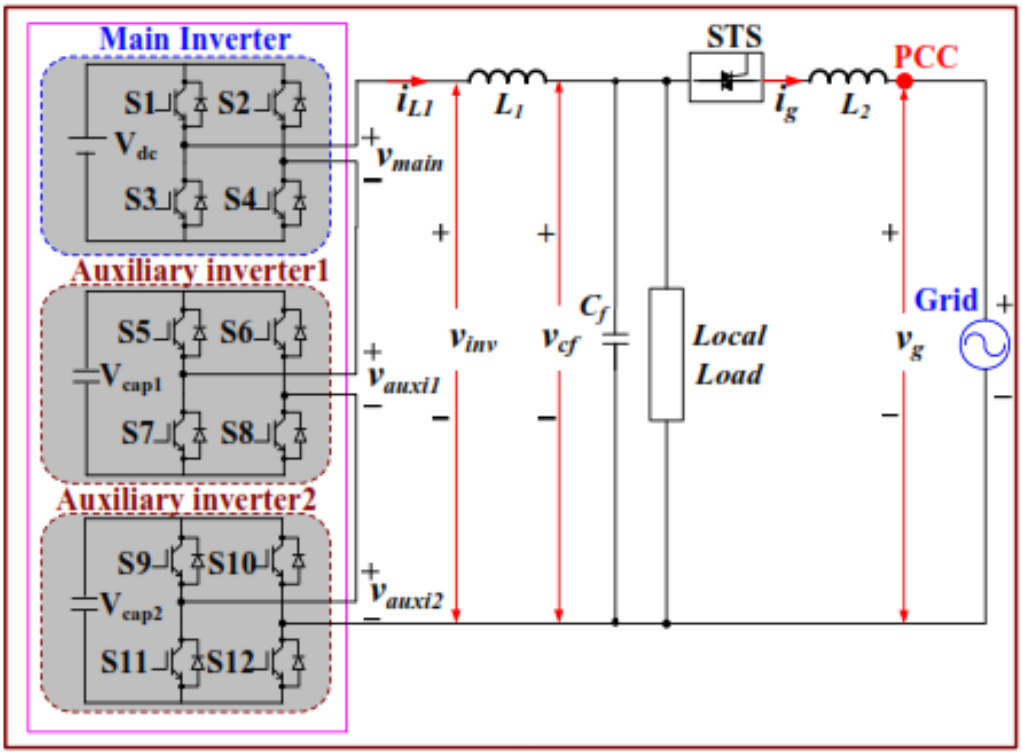


Figure 1- 4 Topology of single-stage GCI

Taken from (Liu, et al., 2010)

1.3.2 Techniques for energy storage

Energy storage systems (ESS) can be traced back to early last century when power generation was often shut down overnight because power electronics control technology was not available (Baker & Collinson, 1999) (Suberu, et al., 2014) (Chen, et al., 2009). Initially, the commonly used ESS approach for peak-shaving in practical applications was hydroelectric pumped storage (HPS). With the technical development of storage, there are variety of storage media, including HPS, compressed air, flywheel, battery, flow battery, capacitor or supercapacitor, superconducting magnet, solar fuels and thermal energy storage (Luo, et al., 2015) (Kousksou, et al., 2014) (Rodrigues, et al., 2014) (Abdin, et al., 2015).

In recent years, integrating ESS into distributed generation systems has attracted many researchers' attention, associated with high penetration of renewable energy generation with unpredictable power fluctuation. These ESS especially include battery systems technology, which is the most widespread energy storage device for power applications. Batteries can be configured in different sizes with wide capacities ranging from watt-hours to gigawatt-hours (Aneke & Wang, 2016). There are many articles proposing a variety of applications aimed at mitigating fluctuation, balancing intermittency of wind or other renewables and RPC, by means of installing a central ESS close to the electrical substation (Suberu, et al., 2014) (Chicco & Mancarella, 2009) (Chen, et al., 2009).

1.4 Major contributions

1.4.1 GCI output with RPC

The thesis describes a novel algorithm, based on D-Q theory, to split the active and reactive currents, to quantitatively control active and reactive power for GCI.

1.4.2 Interleaved bi-directional DC/DC converter for charging/discharging battery

In order to reduce the ripple of converter current and improve thermal dissipation issue, the thesis presents a topology of four-phase interleaved bi-directional DC/DC boost/buck converter (IDBBBC) for charging/discharging battery.

1.4.3 MRes dissertation and publications

1. Fan, Z. & Liu, X., 2015. Smart Inverter with Active Power Control and Reactive Power Compensation. Journal of Electrical and Electronic Engineering, pp. 139-145.
2. Fan, Z., 2012. Mathematical Modelling of Grid Connected Fixed-Pitch Variable-Speed Permanent Magnet Synchronous Generators for Wind Turbines, Preston: UCLAN.
3. Fan, Z. & Liu, X., 2012. A novel universal voltage sag detection algorithm. Power Engineering and Automation Conference (PEAM), *IEEE publisher*.
4. Wen, C., Lu, G., Wang, P., Li, Z., Liu, X., Fan, Z., 2011. Vector control strategy for small-scale grid-connected PMSG wind turbine converter *Innovative Smart Grid Technologies (ISGT Europe) conference, IEEE publisher*.
5. Fan, Z. & Liu, X., *Reactive power compensation for single-phase inverter in microgrid* submitted to International Journal of Advanced Engineering Research and Science to be reviewed.

1.5 Outline of the thesis

The structure of the thesis is as follows: In order to demonstrate methodologies and algorithms, simulations and experiments have been carried out which require specific software tools and hardware development kits to support them.

Chapter 2 describes the software tools, integrated development environment (IDE), the hardware development kit and mathematical tools.

Chapter 3 describes the step-by-step procedures on how to design a SOGIPLL for an embedded real time system and an algorithm, which is demonstrated through MATLAB/Simulink modelling and hardware implementation. PLL as a fundamental function for GCI plays a key role for an on-grid system.

Chapter 4 describes in detail the design of a three-phase SVPWM rectifier through constructing a pair of orthogonal signals for single-phase current, adopting Clarke's and Park's transformation into a single-phase system to split active and reactive current for a single-phase system. The modelling of both three-phase and single-phase rectifiers, and experimental work based on a three-phase SVPWM rectifier are conducted.

Chapter 5 describes the modelling of a four-phase, bi-directional, interleaved, boost/buck DC/DC converter, which can be an ideal charging/discharging converter for the battery storage in a micro-grid.

Chapter 6 presents a smart dispatchable GCI with RPC and the simulation model of multi-inverters synergistically providing RPC for a micro-grid.

Chapter 7 concludes the project with discussion of the project outcomes and briefs future research directions.

Chapter 2 Experimental Environment

2.1 Introduction

In order to achieve power flow bi-directionally in a micro-grid, some key factors must to be taken into account for building an experimental environment for a three-phase system achieve rectifier, based on a GCI topology. Another experimental environment for a single-phase GCI built to demonstrate multi-inverters operating synchronously in a stand-alone system without grid support.

Because the purpose of the rectifier is to achieve bi-directional power flow based on the inverter topology, Figure 2-1 illustrates a bi-directional rectifier/inverter topology in three-phase system consisting of 6 switching devices, if swapping the input and output in the figure, the system can be considered as the conventional three-phase inverter. This requires 6 PWM signal channels, and 3 sampling of phase voltages, and currents and 1 of DC bus voltage, totally requiring 7 channels of analogue to digital (AD) signal conversion. Another issue which has to be considered is to minimise filter inductance size before output by increasing the PWM signal frequency. Moreover, the algorithms for a three-phase SVPWM rectifier system contain complex trigonometrical functions and proportional-integral-derivative (PID) control which require mathematical floating point calculations. Therefore, a high speed TMS320F28335 processor with built-in floating-point unit was utilised to implement the three-phase AC/DC rectifier system.

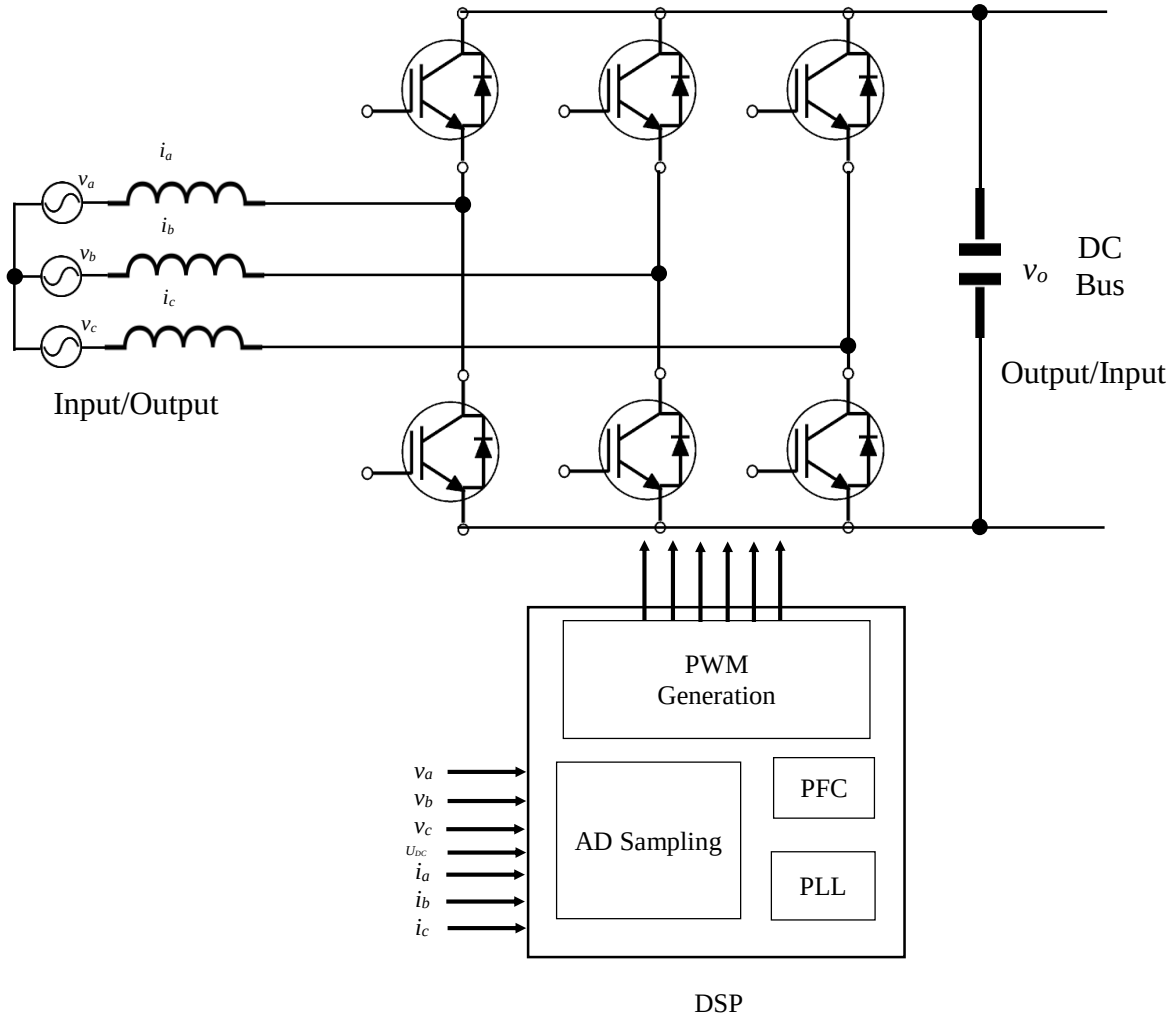


Figure 2- 1 Structure of bi-directional three-phase rectifier/inverter topology

Digital Signal Processor (DSP) TMS320F28335 is a high-performance real-time controller with single-precision Floating-Point Unit (FPU) from Texas Instruments (TI). TMS320F28335 has a good number of peripheral ports, such as 18 PWM outputs and 16 channels 12-Bit ADC.

The C2000 Solar Inverter Development Kit (SDK) shown in Figure 2-2 is designed to achieve the general functions of a GCI. There are some special functions required by the thesis which need extra hardware to support them, such as inverter outputs synchronised with each other when operating in off-grid mode. Therefore, the control board has been re-designed by the author, as shown in Figure 2-4, to replace the original control board SDK shown in Figure 2-

3, using A LPC2132 NXP ARM microcontroller control the main board of the *C2000*™ SDK and this is utilised to implementing a single-phase inverter controlled by a central controller, implemented on a LPC2132 development board, illustrated in Figure 2-5.

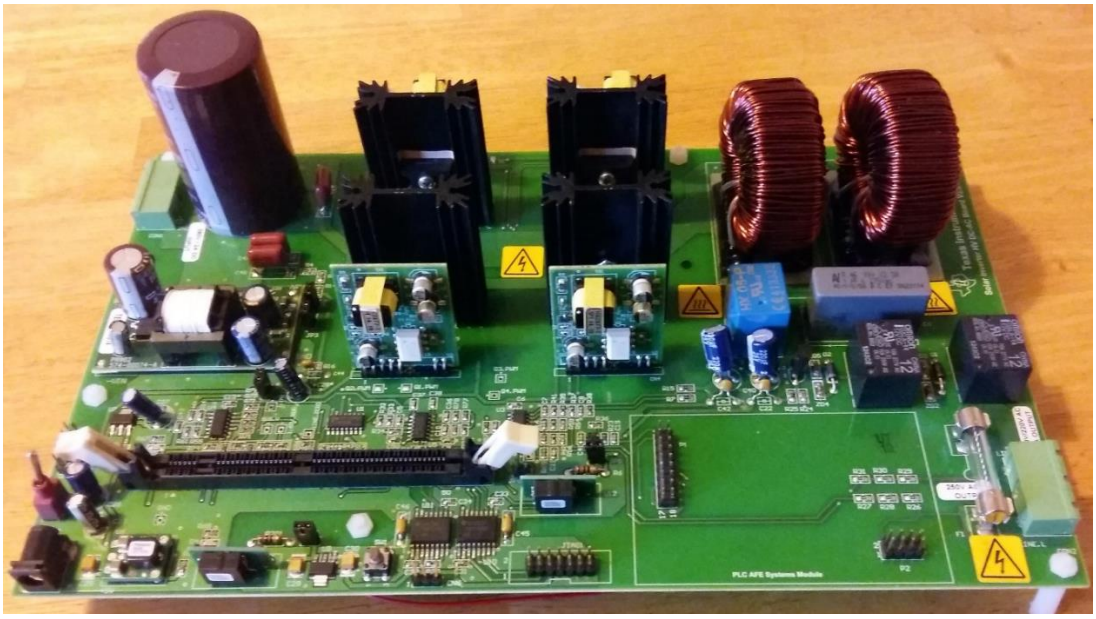


Figure 2- 2 The main board of *C2000*™ SDK

Figure 2- 3 Control board of *C2000*™SDK

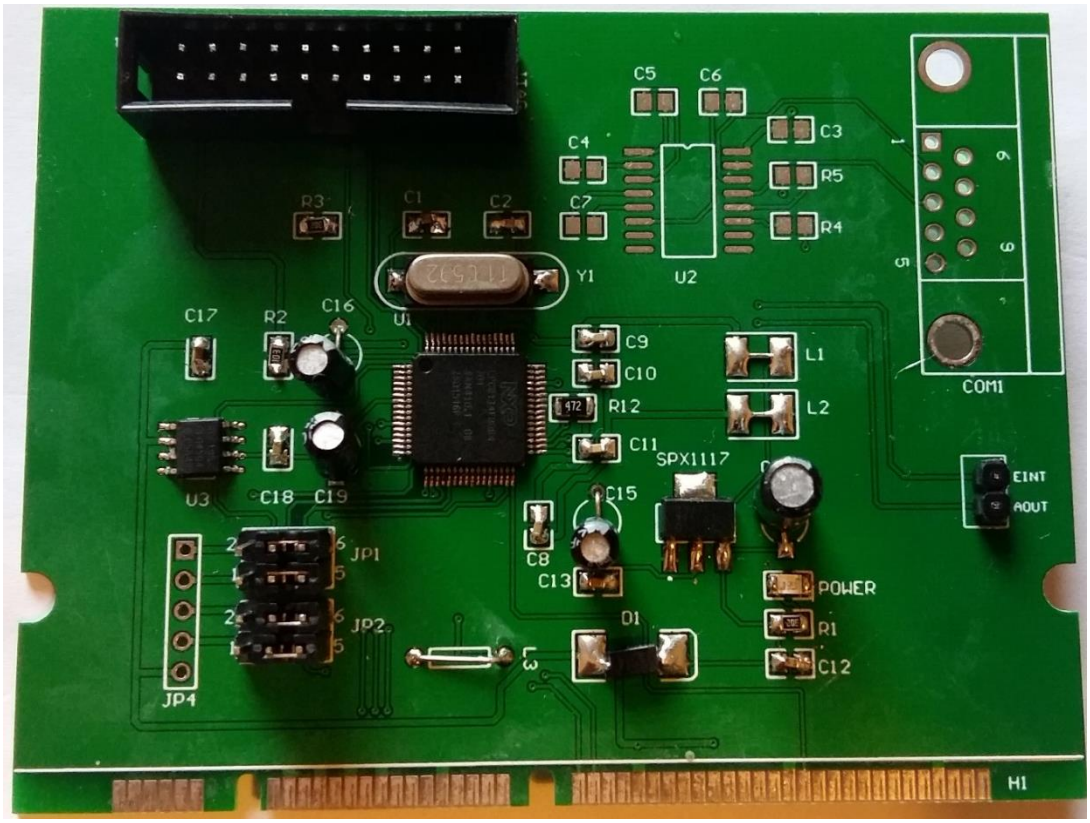


Figure 2- 4 Re-designed control board

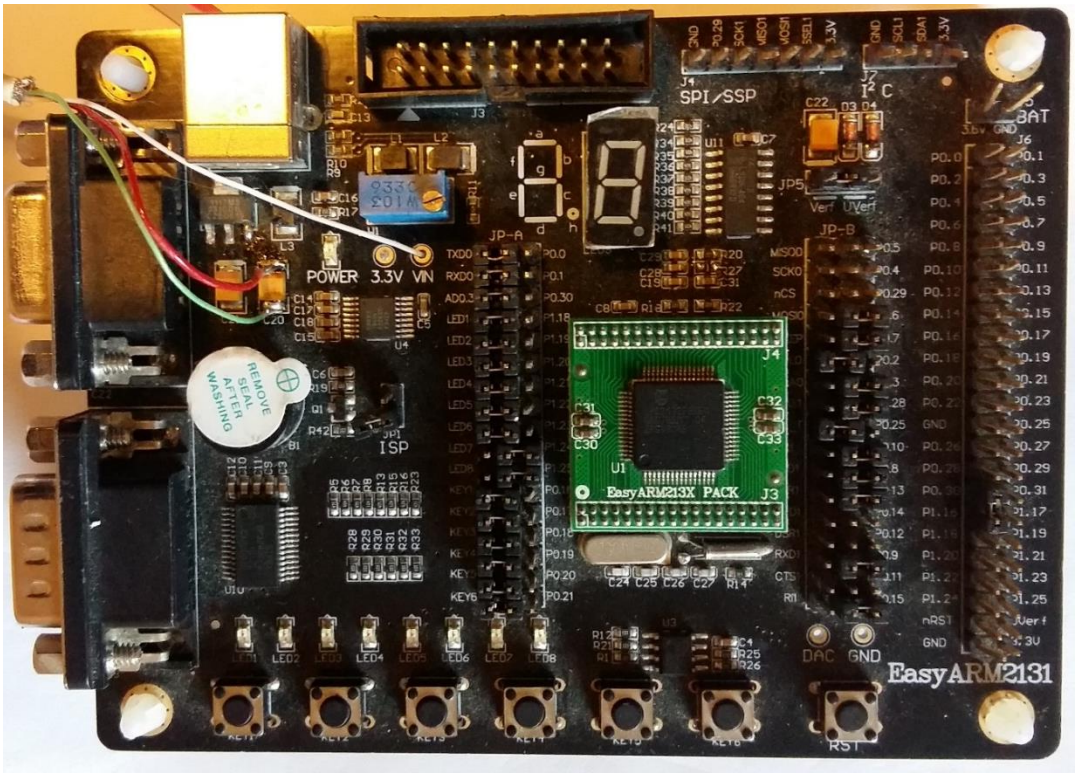


Figure 2- 5 Central control board

C/C ++ was employed to program the controllers using CCS3.3 IDE and Keil uVision 4.0 for the TI DSP processor and ARM microcontroller respectively. All simulations in this thesis were modelled in MATLAB/ SIMULINK; part of the algorithms have been conducted through experiments, such as SVPWM rectifier in three-phase system. Three GCI operate in stand-alone mode.

2.2 Hardware environment

2.2.1 C2000 Solar PV inverter development board

Figures 2-2 and 2-3 show the *C2000*™ SDK is a development platform based on a DSP C2000 Microcontroller from Texas Instruments. The Development Kit is a general and conventional inverter, which is insufficient to provide communications between the inverter and a central controller. Therefore, the circuit of the control part of the Inverter Development Kit was redesigned and the C2000 Microcontroller replaced by a NXP LPC2132 ARM microcontroller to implement the function of a standalone inverter, which was used to demonstrate the feasibility of solving synchronising issues under circumstances of multi-inverter operate in off-grid mode. In the experiment, only three inverters connected together operate in off-grid mode.

2.2.2 NXP LPC 2132 ARM

The LPC2132 microcontroller is based on a 16/32-bit ARM7TDMI-S control processor unit (CPU) with real-time emulation and embedded trace support and a 64kB embedded high-speed flash memory. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at maximum clock rate. LPC2132 has 6 channels of PWM and 8 channels of 10-Bit A/D converter which are sufficient to implement a single-phase full-bridge inverter.

2.2.3 TMS320F28335 DSP

TMS320F28335 is a high-performance static CMOS (Complementary Metal-Oxide Semiconductor) technology with speed up to 6.67ns cycle time. The total harmonic distortion

(THD) is inversely proportional to the switching frequency of the rectifier/inverter-bridge, which means using a high-speed DSP to implement active rectifier with PFC or GCI, which has the features of high reliability and power quality.

Enhanced control peripherals include 18 PWM outputs and 16 channel AD converters with 12-Bits resolution and 80ns high speed sampling rate. The most prominent feature of the F28335 DSP is that it has an excellent floating point, built-in coprocessor.

2.2.4 Insulated-gate bipolar transistor (IGBT)

An IGBT FF75R12RT4 shown in Figure 2-6 was utilised to build the three-phase rectifier/inverter-bridge; it is 34mm module with fast Trench/Fieldstop IGBT4 and Emitter Controlled 4 diodes, produced by Infineon. The voltage stresses of FF75R12RT4 between collector and emitter is up to 1200V, continuous DC maximum collector current is 75A and maximum repetitive peak collector current is 150A. The maximum turn-on and turn-off delay times are 0.15μs and 0.40μs respectively for inductive loads (MK, 2013-11-05).

Figure 2- 6 IGBT FF75R12RT4

2.2.5 Voltage and current transducers

TBC50SYH was chosen to measure three-phase rectifier current due to its 50A nominal current rating. The TBC-SYH series high-precision current sensor is a closed loop device based on Hall Effect, with a galvanic isolation between primary and secondary circuit. It has strong anti-jamming ability and can provide accurate electronic measurement of DC, AC or pulsed currents.

The TLP7820 optically isolated amplifier was used to measure voltage, using a delta-sigma AD converter input circuit and providing an analogue output via a 1 bit D/A and a low pass filter. Figure 2-7 shows sampling of an input voltage.

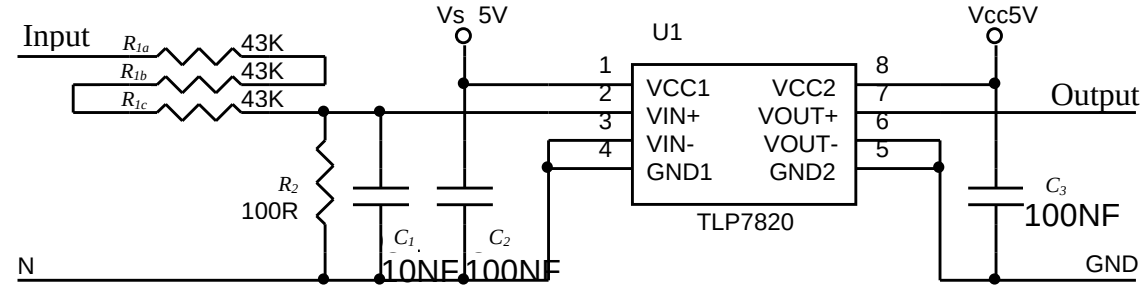


Figure 2-7 Sampling circuit of input voltage

The TLP7820 device, which is shown in Figure 2-8, can detect small current and voltage fluctuations with high-precision. It offers a common-mode transient immunity of 15kV/μs minimum, enabling stable operation in electrically noisy environments.

Figure 2- 8 TLP7820 device

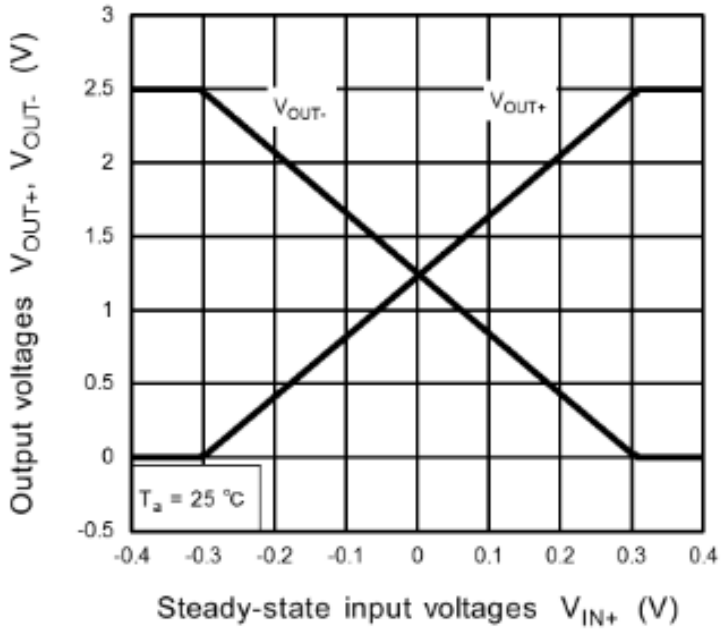


Figure 2- 9 Linear relationship between input and output of TLP7820

According to the datasheet of the TLP7820, the analogue input voltage is limited between -300 mV +300 mV as shown in Figure 2-9. Assuming a maximum input the AC peak voltage of $300 \times \sqrt{2}$V, this must then be attenuated to 300mV. According to Figure 2-7, the gains G_s of sampling input voltage can be obtained in the following equation:

$$G_S = \frac{R_2}{R_{1a} + R_{1b} + R_{1c} + R_2} = 7.7459 \times 10^{-4} \qquad (2-1)$$

Because the TLP7820 output signal is limited -300mV and +300mV without an amplifier, an additional stage of amplification with a gain of 10 was added between the output and sampling input, as shown in Figure 2-10.

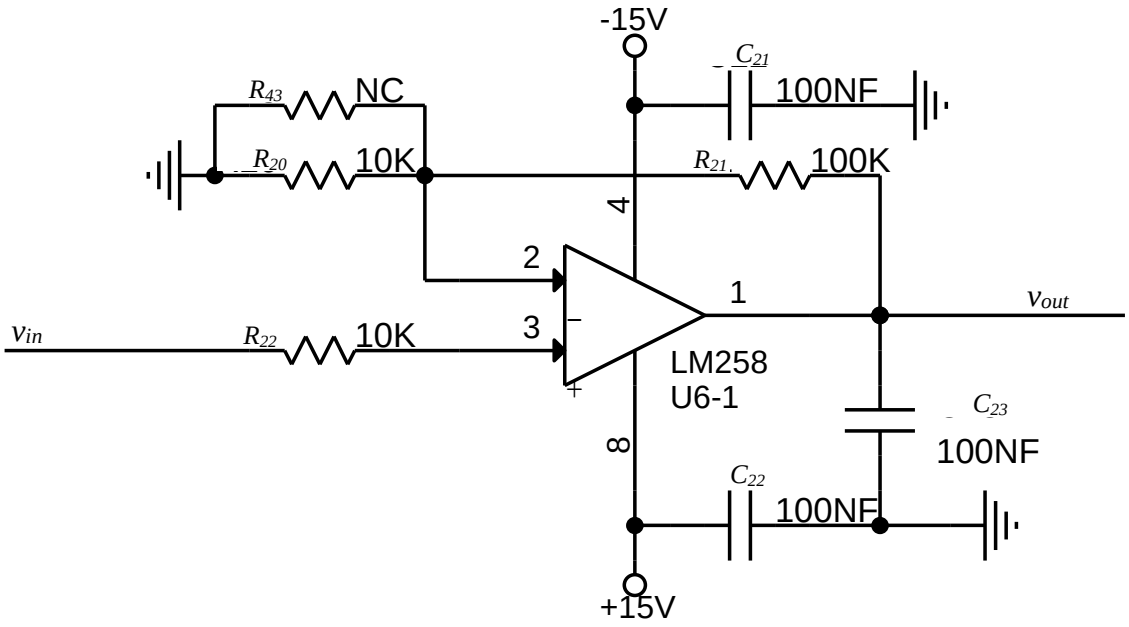


Figure 2- 10 Sampling Gain

2.3 Software environment

2.3.1 MATLAB/Simulink

Simulink is a user friendly block diagram environment for simulation and Model-Based design, supporting simulation, automatic code generation, and continuous test and verification of embedded systems.

Simulink provides a graphical editor, customizable block libraries, and solvers for modelling and simulating dynamic systems. It is integrated with MATLAB, enabling incorporation of MATLAB algorithms into models and exportation of simulation results to MATLAB for further analysis.

2.3.2 Keil uVision

The MDK-ARM is a complete IDE for Cortex-M, Cortex-R4, ARM7 and ARM9 processor based devices. It is specifically designed for microcontroller applications with easy to use and

powerfully adequate for most embedded applications. Therefore, MDK-ARM was chosen to program the central control system using C/C++ language.

2.3.3 Code composer studio

Code composer studio (CCS) is an IDE that supports TI's Microcontroller and Embedded Processors portfolio and comprises a suite of tools used to develop and debug embedded applications. CCS has resources to help developers, which can shorten development cycles and reduce development costs and improve development efficiency. The technology of Real-time Exchange Data (RTXD) was developed by TI, and gives designers continuous, real-time visibility into their applications. The bi-directional capability allows developers to access data from the application for real-time visibility, or to simulate data input to the DSP, perhaps before real-time sensor hardware is available.

In Simulink, the accuracy of results of simulation depends on the time step interval (The Math Works 2011). In general, the smaller the time step, the more accurate the simulated results. In the case of variable-step solvers, the solver can automatically determine the time step; in the case of fixed-step solvers, the time step can be specified. Therefore, the results of simulation based on MATLAB/Simulink have some tolerances compared with ideal mathematical models.

2.4 Mathematical methods

2.4.1 Clarke's transformation

Clarke's Transformation as shown in Figure 2-11. Considering a vector X (x_a, x_b and x_c), *a*-, *b*- and *c*- are the component vectors in directions *a*, *b* and *c*, respectively, in the static three-phase system. x_α and x_β are α- and b-component vectors of X in the stationary two-phase frame $\alpha\beta$ respectively. As Figure shows, the vector X in three-phase system can be expressed in stationary two-phase frame.

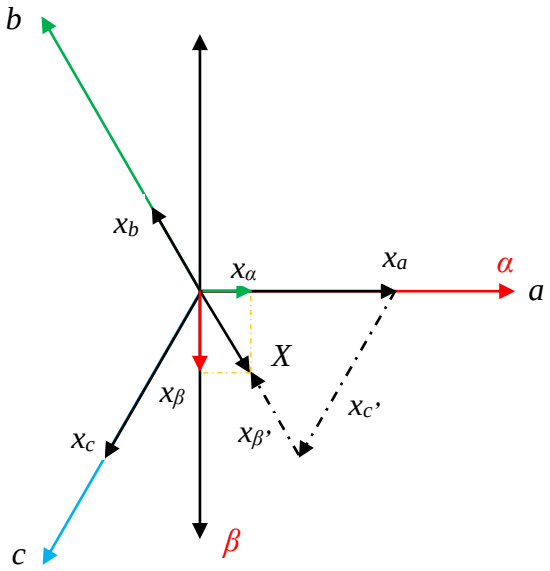


Figure 2 - 11 Clarke's Transformation

The voltages of a three-phase balanced system can be written as the following mathematical model:

$$\begin{cases} v_a = v_{max}\cos\omega t \\ v_b = v_{max}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c = v_{max}\cos\left(\omega t - \frac{4\pi}{3}\right) \end{cases} \tag{2-2}$$

Let

$$v_\alpha = v_{max}\cos\omega t$$

And the orthogonal variable of v_α be v_β, so that:

$$v_\beta = v_{max}\sin\omega t$$

Adopting v_α and v_β to simplify Equation (2-2) as follows:

$$v_a = v_\alpha \tag{2-2.1}$$

$$v_b = v_{max}(\cos\omega t\cos\frac{2\pi}{3} + \sin\omega t\sin\frac{2\pi}{3})$$

$$= -\frac{1}{2}v_\alpha + \frac{\sqrt{3}}{2}v_\beta \qquad (2-2.2)$$

$$v_c = v_{max}(cos\,\omega t\, cos\frac{2\pi}{3} - sin\omega t sin\frac{2\pi}{3})$$

$$= -\frac{1}{2}v_\alpha - \frac{\sqrt{3}}{2}v_\beta \qquad (2-2.3)$$

Therefore, rearranging v_a, v_b and v_c

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = A \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \qquad (2-3)$$

where $A = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}$

2.4.2 Inverter Clarke's transformation

Finding the inverse matrix for the matrix A, then multiplying both sides of Equation (2-3) by the inverse of *A* results in Equation (2-4) giving v_α and v_β.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad (2-4)$$

where,

v_α, v_β are the stationary orthogonal reference frame quantities.

2.4.3 Park's transformation

The two-axis stationary orthogonal reference frame quantities are transformed into a *d-q* rotating reference frame using the Park's transformation as illustrated in Figure 2-12.

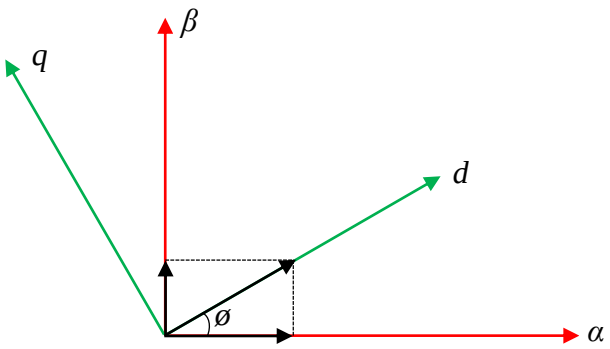


Figure 2- 12 Park's transformation

The rotating reference frame *d*-*q* quantities can be obtained as follows.

$$\begin{cases} v_d = v_\alpha \cos \emptyset + v_\beta \sin \emptyset \\ v_q = v_\beta \cos \emptyset - v_\alpha \sin \emptyset \end{cases} \quad (2-5)$$

where,

v_d, v_q are the rotating reference frame quantities.

v_α , v_β are the stationary orthogonal reference frame quantities.

ø is the rotational angle.

2.4.4 Inverse Park's transformation

Then the Inverse Park's transformation can be expressed as the following equation:

$$\begin{cases} v_\alpha = v_d \cos \emptyset - v_q \sin \emptyset \\ v_\beta = v_q \cos \emptyset + v_d \sin \emptyset \end{cases} \quad (2-6)$$

where,

v_d, v_q are the rotating reference frame quantities.

v_α , v_β are the stationary orthogonal reference frame quantities.

ø is the rotational angle.

2.4.5 P-Q theory

The voltages of a three-phase balanced system can be written as the following mathematical model:

$$\begin{cases} v_{sa} = A_m \cos \omega t \\ v_{sb} = A_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_{sc} = A_m \cos\left(\omega t - \frac{4\pi}{3}\right) \end{cases} \tag{2-7}$$

Through the *d-q* coordinate transformation, the voltage of a three-phase system in the *d-q* rotating frame system can be expressed as:

$$\begin{cases} v_d = A_m \\ v_q = 0 \end{cases} \tag{2-8}$$

According to the instantaneous power of P-Q theory, the three-phase active power *P* and reactive power *Q* can be written in the stationary frame system *αβ* as

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2-9}$$

where v_α ,v_β and i_α, i_β are mutually orthogonal pair of voltages and currents respectively.

Through Park's transformation, Equation (2-9) can be expressed as follows:

$$\begin{cases} P = v_d i_d + v_d i_q cos\omega t(sin\omega t - cos\omega t) \\ Q = -v_d i_q \end{cases} \tag{2-10}$$

In Equation (2-10), as i_q approaches 0 then the reactive power component approaches 0 and only the active power remains, i.e. the term $v_d i_d$. Through analysing the above equation, the reactive power *Q* of the power grid can be controlled by adjusting the instantaneous quadrature component of current i_q in the *d-q* rotating frame.

2.5 Summary

In this chapter, the experimental environment, including hardware, software and programming IDE, are briefly introduced. Mathematical tools, particularly Park's, Clarke's transformation and P-Q theory, are addressed as well. These tools are widely employed in power electronic control algorithm development.

Chapter 3 Phase-Locked Loop

3.1 Introduction

PLLs are common signal processing methods. They are widely used in applications such as measurement, coherent demodulation, time synchronisation, frequency synthesis, and other signal processing fields. There are a number of types of PLL depending on the implementation technology, including analogue PLL (APLL), digital PLL (DPLL), synchronous frame PLL (SFPLL) and soft PLL (SPLL). In the development of virtual radio technology, SPLL has been used widely (Liu, et al., 2007). The basic principle of SPLL is similar to that of conventional PLL, but differs significantly in the mathematical model, parameter design and implementation modalities (Bhardwaj, 2013) (Guo, et al., 2011).

The frequency, phase angle and amplitude of the AC voltage on the electricity grid are critical parameters for a GCI, employed to inject AC power to the grid, to ensure the inverter system operates properly and does not cause grid transients. In order to generate the reference control signals for the PWM control of the inverter switches, accurate detection of the phase angle of the electrical quantities on the grid is essential.

A few topologies of PLL for GCIs have been implemented in industrial applications. The sine and cosine of the phase angle are key parameters for a GCI; conventional methods yield those parameters by firstly obtaining phase angle from the power grid voltage, then through a series triangular computations. Actually, because the grid voltage is a sine signal, obtaining the grid voltage phase angle is unnecessary if a pair of orthogonal signals from a sampling of the sine signal can be obtained. The SOGI can generate a pair of orthogonal signals, therefore a SOGIPLL, with a strong anti-interference PLL algorithm, has been introduced to achieve phase synchronisation with the grid. This technique has been analysed in detail in the analogue

continuous-time domain (Rodriguez, et al., 2009) and the implementation in the digital discrete-time domain is described in this chapter. Finally the results of simulation are presented.

3.2 Generic PLL

Figure 3-1 shows the functional block diagram of a generic PLL, where $ø_i$ and $ø_o$ are the relative phase angles of the input and output voltage signals v_i and v_o. The Phase Detector multiplies the input and output signals and produces a voltage v_d proportional to the phase difference between the input frequency with feedback frequency output , which contains a second harmonic term that need to be removed by the Loop Filter, which is a low-pass filter. The Loop Filter outputs voltage v_{vco} which is proportional to the phase difference $ø_i$ - $ø_o$ and employed to control the Voltage Controlled Oscillator (VCO).

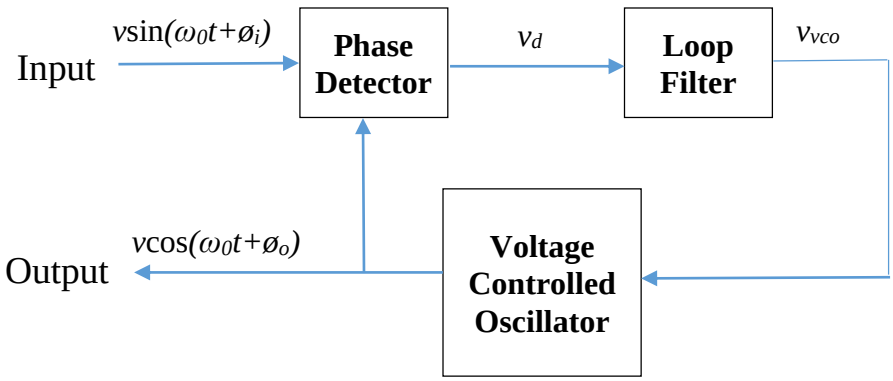


Figure 3- 1 Diagram of generic PLL

A conventional linearised SFPLL block diagram is illustrated in Figure 3-2, which is widely employed in three-phase GCI applications. The instantaneous phase angle $ø$ is detected by synchronising the d-q rotating reference frame with the three-phase electricity grid. When the phase angle is locked to the phase angle of grid voltage vector, the output quadrature component should be 0 and the direct component indicates the grid voltage amplitude.

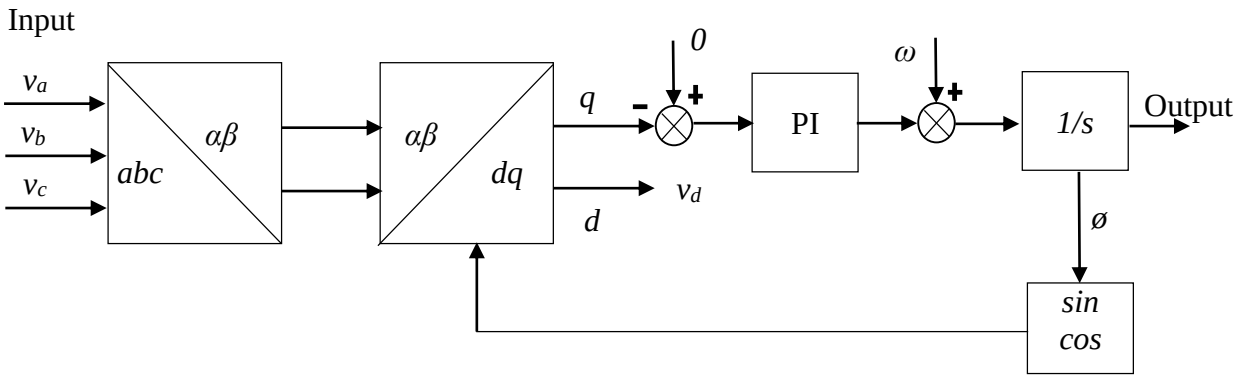


Figure 3- 2 Linearised conventional SFPLL block diagram

3.3 SOGISPLL mathematical model

Figures 3-3 and 3-4 illustrate block diagrams of both open-loop and close-loop implementations of a SOGI, respectively (Fan & Liu, 2015).

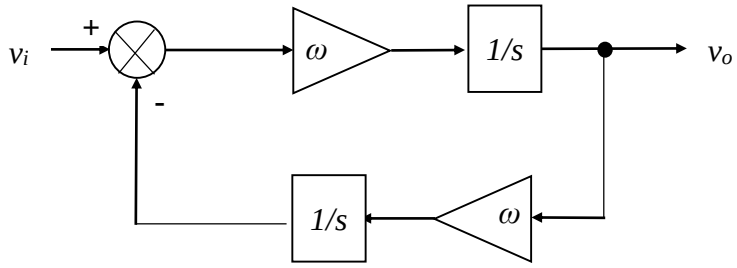


Figure 3- 3 Open-loop system of SOGI

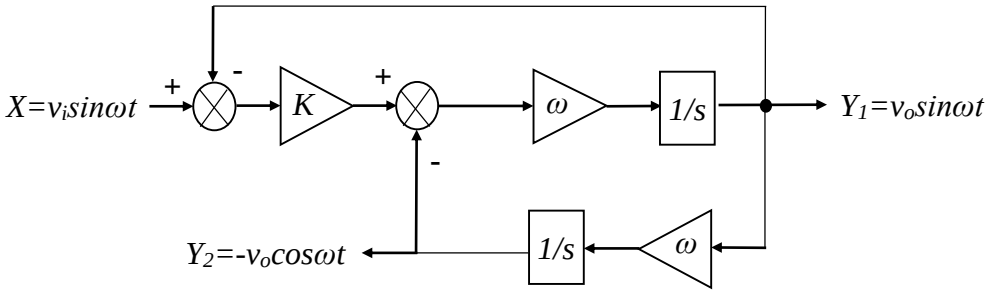


Figure 3- 4 Close-loop system of SOGI

According to the Figures above, let X represent the input signal $v_i sin\omega t$, let Y_1 represent the output signal $v_o sin\omega t$ and Y_2 represent the output signal $-v_o cos\omega t$, then the mathematical model of the close-loop system in the Laplace domain can be expressed as:

$$\begin{cases} Y_1 = \dfrac{(K(X - Y_1) - Y_2)\omega}{s} \\ Y_2 = \dfrac{Y_1\omega}{s} \end{cases} \qquad (3-1)$$

where,

K is the gain which affects the speed of response and the bandwidth of the close-loop system,

ω is the signal frequency in radians, and

$\frac{1}{s}$ is the integrator in Laplace domain.

Substituting $\frac{Y_1\omega}{s}$ for Y_2 and rearranging Equation (3-1) yields:

$$\begin{cases} Y_1 = \dfrac{K\omega sX}{s^2 + K\omega s + \omega^2} \\ Y_2 = \dfrac{K\omega sX}{s^2 + K\omega s + \omega^2} \cdot \dfrac{\omega}{s} \end{cases} \qquad (3-2)$$

So the transfer function of the close-loop system can be obtained as:

$$\begin{cases} H_{s1} = \dfrac{Y_1}{X} = \dfrac{K\omega s}{s^2 + K\omega s + \omega^2} \\ H_{s2} = \dfrac{Y_2}{X} = \dfrac{K\omega^2}{s^2 + K\omega s + \omega^2} \end{cases} \qquad (3-3)$$

Converting the denominators to the standard second order form:

$$s^2 + 2\zeta\omega s + \omega^2 \qquad (3-4)$$

where, ζ is the damping factor (typically ζ=1/√2=0.707), so in the term of denominator of Equation (3-3), $K = 2\zeta = 1.414$ and the frequency of the electricity grid is 50 Hz, which means $\omega = 2\pi 50$ rad/s.

Figure 3-5 illustrates the step responses of the system with the gain of *K*= 0.5, 1.2, 1.414, 2 and 3 respectively. These responses show that the system reaches steady state conditions, and the shortest time is 0.0247s when the gain K = $2\zeta = \sqrt{2}$ (i.e. $\zeta = \frac{1}{\sqrt{2}}$), as the response in red on the graph below.

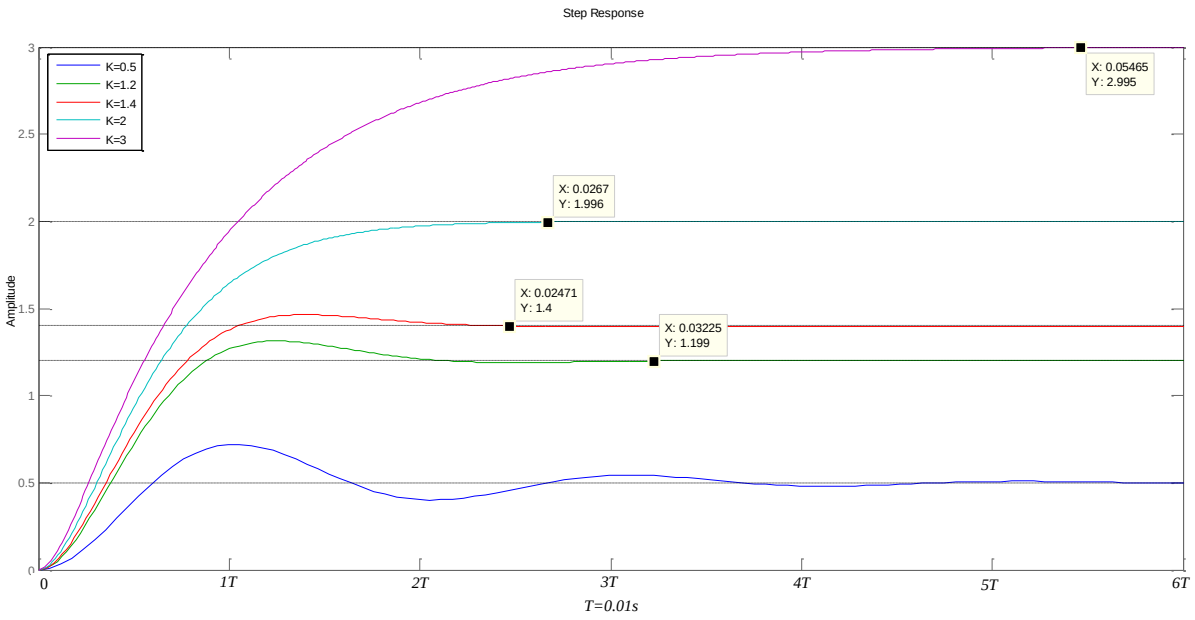


Figure 3- 5 Step responses of a closed-loop SOGIPLL in continuous-time

Equation (3-3) is the transfer function of the close-loop system in continuous-time in the Laplace domain. The equivalent discrete-time transfer function is required to implement the second order integrator in a digital signal system. There are a number of methods that can be employed to obtain the discrete-time approximation of a continuous-time transfer function, such as Forward Difference, Backward Difference, Tustin's Approximation and Bilinear Transformation. (Ogata, 1995).

Tustin's approximation, also known as Euler's method or Trapezoidal Approximation, (Ciobotaru, et al., 2006) is a common method and is demonstrated below using the substitution $\frac{2}{T}\frac{z-1}{z+1}$ to replace the Laplace operator *s*.

$$H_{s1} = \frac{Y_1}{X} = \frac{K\omega s}{s + K\omega s + \omega^2} = \frac{444.2208s}{s^2 + 444.2208s + 98696.044}$$

Substituting $\frac{2}{T}\frac{z-1}{z+1}$ for the Laplace operator for *s* and sampling time 2e-5s for *T*, results in

$$H_{z1} = \frac{444.2208\frac{2}{2\times10^{-5}}\frac{z-1}{z+1}}{\left(\frac{2}{2\times10^{-5}}\frac{z-1}{z+1}\right)^2 + 444.2208\frac{2}{2\times10^{-5}}\frac{z-1}{z+1} + 98696.044}$$

This result simplifies to

$$H_{z1} = \frac{0.004423z^2 - 0.004423}{z^2 + 1.991z + 0.9912} \qquad (3-5)$$

$$H_{s2} = \frac{Y_2}{X} = \frac{K\omega^2}{s^2 + K\omega s + \omega^2} = \frac{139556.21}{s^2 + 444.2208s + 98696.044}$$

Substituting the Laplace operator *s* with $\frac{2}{T}\frac{Z-1}{Z+1}$ and sampling time *T* with 2e-5s

$$H_{z2} = \frac{139556.21}{\left(\frac{2}{2\times10^{-5}}\frac{z-1}{z+1}\right)^2 + 444.2208\frac{2}{2\times10^{-5}}\frac{z-1}{z+1} + 98696.044}$$

On rearrangement this becomes

$$H_{z2} = \frac{1.389\times10^{-5}\,z^2 + 2.779\times10^{-5}z + 1.389\times10^{-5}}{z^2 + 1.991z + 0.9912} \qquad (3-6)$$

MATLAB's c2d command can also be utilised to convert continuous to discrete transfer function as in the following example.

```
>> W=2*pi*50;
>> K=1.414;
>> H1=tf([K*W 0],[1 K*W W*W])

H1 =

          444.2 s
  ----------------------
  s^2 + 444.2 s + 9.87e04

Continuous-time transfer function.

>> HD1=c2d(H1,2e-5,'tustin')

HD1 =

  0.004423 z^2 - 0.004423
  -----------------------
  z^2 - 1.991 z + 0.9912

Sample time: 2e-05 seconds
Discrete-time transfer function.


>> W=2*pi*50;
>> K=1.414;
>> H2=tf(K*W*W,[1 K*W W*W])

H2 =

         1.396e05
  ----------------------
  s^2 + 444.2 s + 9.87e04

Continuous-time transfer function.

>> HD2=c2d(H2,2e-5,'tustin')

HD2 =

  1.389e-05 z^2 + 2.779e-05 z + 1.389e-05
  ---------------------------------------
          z^2 - 1.991 z + 0.9912

Sample time: 2e-05 seconds
Discrete-time transfer function.
```

The MATLAB results and the results produces by Tustin's Approximation are the same.

3.4 Discrete Implementation of SOGIPLL

Equations (3-5) and (3-6) show that the SOGIPLL system response functions are second-order digital filters with feedback. Hence, they can be achieved using an infinite impulse response (IIR) digital filter. The standard form of a digital second order IIR filter is shown below:

$$H_d(Z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}$$

where b_0, b_1 and b_2 are feed-forward coefficients

a_0, a_1 and a_2 are feed-back coefficients

Figure 3-6 shows a general block diagram of the digital second order IIR filter in Direct Form II structure.

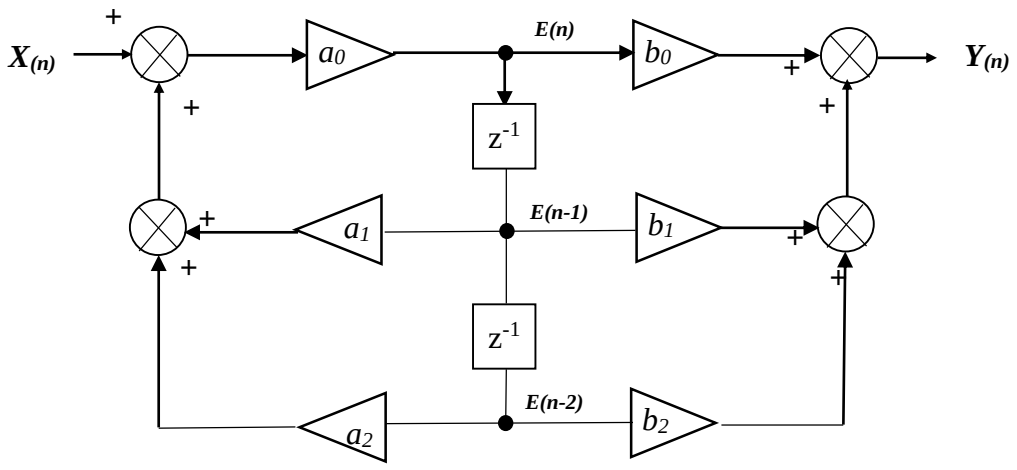


Figure 3- 6 Direct Form II structure for IIR filter

where the Z^{-1} blocks represent a single sample delay and the nodes $E_{(n)}$, $E_{(n-1)}$ and $E_{(n-2)}$ represent memory for temporary storage during the calculations.

The Equations of the discrete transfer function, (3-5) and (3-6), can be written as the relationship between instantaneous input and output as follows:

$$H_{z1} = \frac{v_{o(n)}}{v_{i(n)}} = \frac{Y_{1(n)}}{X_{(n)}} = \frac{0.004423z^2 - 0.004423}{z^2 + 1.991z + 0.9912} \quad (3-7)$$

$$H_{z2} = \frac{v_{o(n)}}{v_{i(n)}} = \frac{Y_{2(n)}}{X_{(n)}} = \frac{1.389z + 2.779 \times 10^{-5}z + 1.389 \times 10^{-5}}{Z^2 + 1.991z + 0.9912} \quad (3-8)$$

where $v_{i(n)}$ is the system discrete input and $v_{o(n)}$ is the system discrete output.

Multiplying the numerator and denominator by z^{-2} and solving for instantaneous output $Y_{1(n)}$. For Equation (3-7) this gives.

$$(1+1.991z^{-1}+0.9912z^{-2})Y_{1(n)} = (0.004423-0.4423z^{-2})X_{(n)}$$

Which yields

$$Y_{1(n)} = 0.004423X_{(n)}-0.4423z^{-2}X_{(n)}-1.991Z^{-1}Y_{1(n)}-0.9912z^{-2}Y_{1(n)}$$

According to $X_{(n)}z^{-k} = X_{(n-k)}$ and $Y_{1(n)}z^{-k} = Y_{2(n-k)}$, rearranging the equation above gives

$$Y_{1(n)} = 0.004423X_{(n)}-0.4423X_{(n-2)}-1.991Y_{1(n-1)}-0.9912Y_{1(n-2)} \quad (3-9)$$

Now for Equation (3-9), multiplying the numerator and denominator by z^{-2} and solving for instantaneous output $Y_{2(n)}$ gives.

$$(1+1.991z^{-1}+0.9912z^{-2})Y_{2(n)} = (1.389\text{x}10^{-5}+2.779\text{x}10^{-5}z^{-1}+1.389\text{x}10^{-5}z^{-2})X_{(n)}$$

Substituting $X_{(n)}z^{-k} = X_{(n-k)}$ and $Y_{2(n)}z^{-k} = Y_{2(n-k)}$, and rearranging gives

$$Y_{2(n)} = 1.389\text{x}10^{-5}X_{(n)}+2.779\text{x}10^{-5}X_{(n-1)}+1.389\text{x}10^{-5}X_{(n-2)}- 1.991Y_{2(n-1)}-$$

$$0.9912Y_{2(n-2)} \quad (3-10)$$

3.5 Simulation

The Simulink model created by utilising MATLAB/Simulink according to Equations (3-9) and (3-10) is illustrated in Figure 3-7. A random white noise generator is added at the input terminal to test the stability and anti-interference capability of the system. In a practical system, the

sampling accuracy of the analogue to digital signal converter is affected by noise and/or system drift.

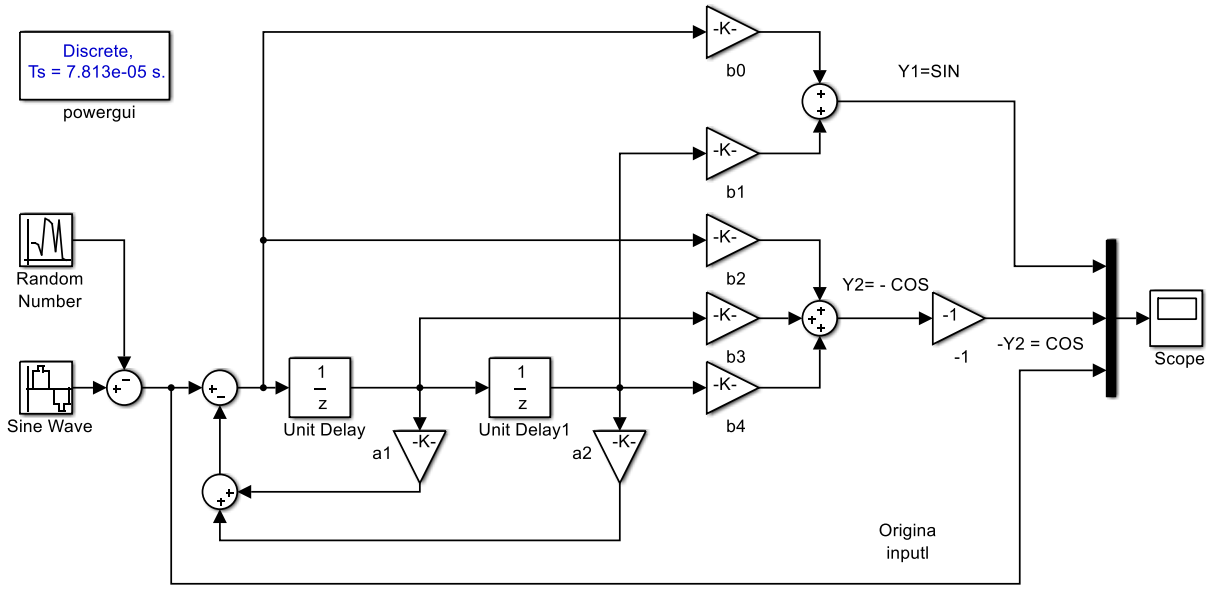


Figure 3- 7 Simulink model of SOGIPLL

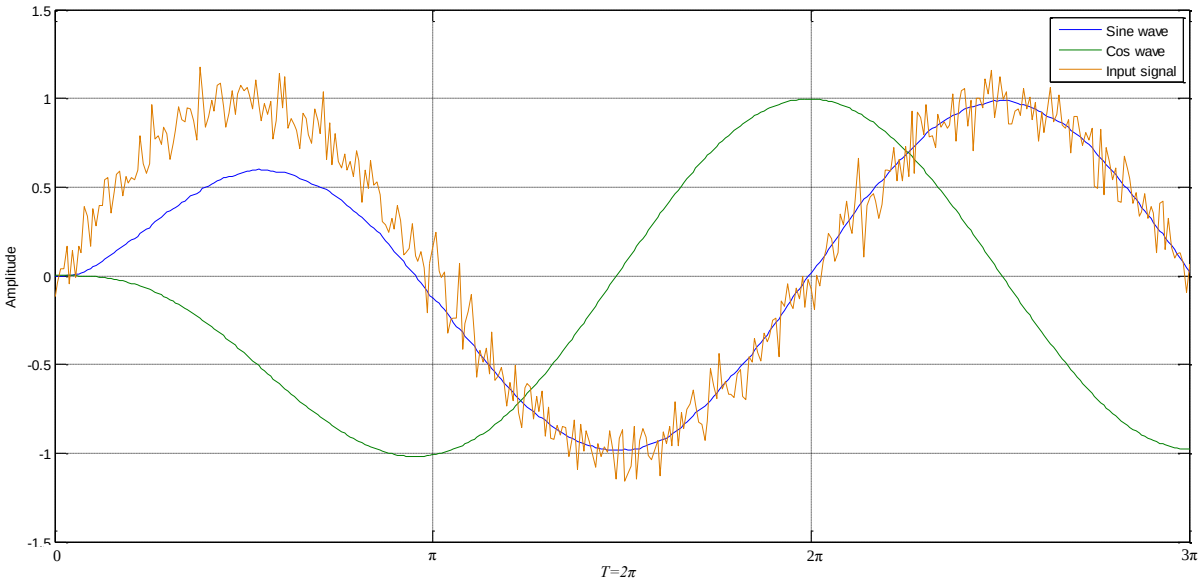


Figure 3- 8 Comparison between input with white noises and PLL output

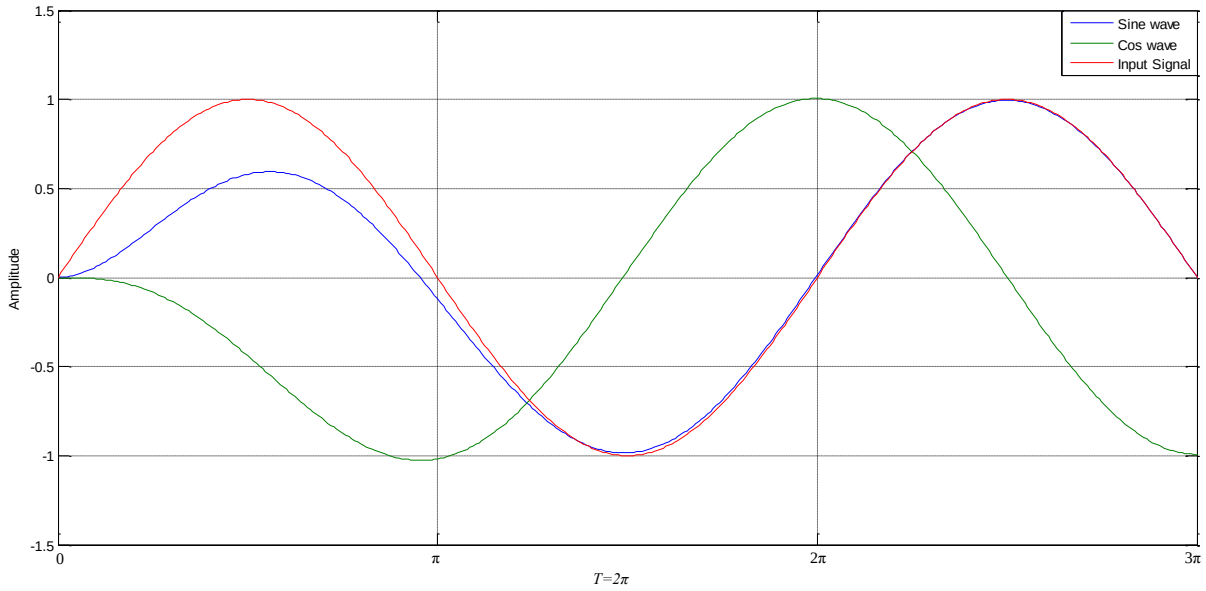


Figure 3- 9 Comparison of original input and PLL output

Figure 3-8 shows that the output of the SOGIPLL has anti-interference performance when random white noise is added to an input signal with 50 Hz frequency. Additionally, Figure 3-9 shows the sine (blue line) and cosine (green line) generated by the SOGIPLL follows the original input signal (red line) after one periods, the difference between the output (blue line) and the input (red line) wave has decreased to negligible levels.

3.6 Summary

The simulation results demonstrate that SOGI orthogonal output signals with anti-interference performance can be employed to implement PLL in a GCIS. In addition, SOGI only requires one input signal, which means the model can be applied in both single-phase and three-phase GCIs.

Chapter 4 AC to DC Rectifier

4.1 Introduction

A Three-phase SVPWM rectifier has attractive characteristics including controllable DC output voltage, low THD, high power factor for the grid current (Zheng, et al., 2010), and bi-directional power flow, which are the major features considered in this thesis.

Rapid growth of renewable power generation in the past decade has certainly been facilitated advanced inverter technology development, which plays a key role in interfacing renewable power generators with the power grid. The most popular three-phase inverter circuit consists of six IGBT switches in a full-bridge configuration, because IGBT has relative higher voltage and current rating. The single-phase inverter circuit is formed by four IGBT switches in a full-bridge.

The full-bridge topology composed of IGBTs or MOSFETs not only utilities to inverter DC voltage into power grid, it also can implement an active controllable rectifier.

Because each switching devices in full-bridge circuit is equipped with an anti-parallel, flywheel diode to protect the device if the load is inductive, as all the switching devices without PWM control signals the full-bridge circuit could be operated in the uncontrollable rectifier mode, because of each switching device has flywheel diode connected in shunt.

As using PWM signals to control switching devices, then the full-bridge topology could be operated in active controllable rectifier or inverter mode, which depends on different control algorithms.

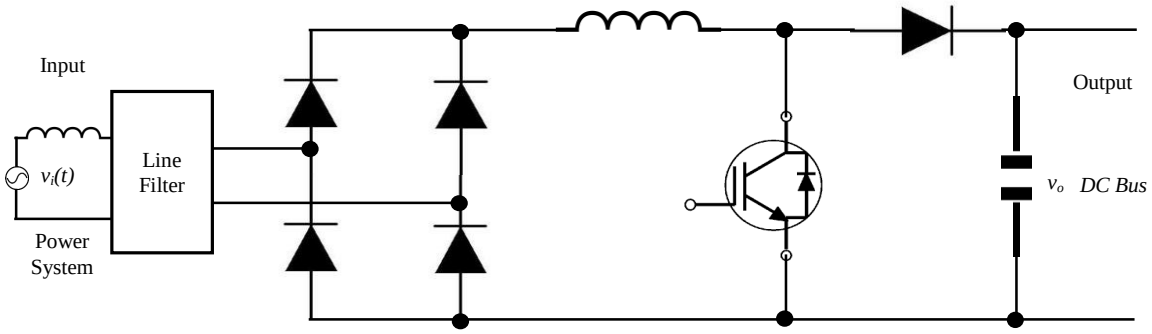
During off-peak or low-tariff hours for peak-hour or high-tariff hours use, integrating energy storage on the DC bus link to store power from grid has great potential advantage.

Conventional renewable energy GCI interfaces to the power grid with as much renewable generator power output as it can deliver but does not offer RPC, which is normally provided by dedicated local reactive power or is matched by the reactive capability of synchronous generators in large power stations.

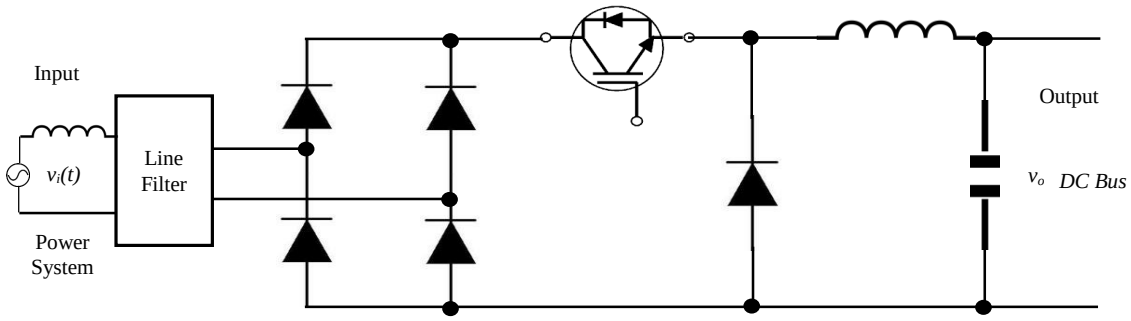
For a load centre, it is a general practice to compensate reactive power demand from the load centre at the PCC so as to maintain a statutory voltage at the PCC and the distribution network and minimise the line loss. Large synchronous generators are required to produce reactive power, because transmission lines demand reactive power in addition to that needed at distribution load centres. For a more distributed power generation system, it would be ideal that all generation units share the responsibility of providing reactive power.

There are a number of topologies presented to implement active rectifiers with PFC, such as the buck rectifier, boost rectifier, buck-boost rectifier, H-bridge converters (Rodriguez, et al., 2016), and Vienna rectifier (Kedjar, et al., 2014; Shaon & Salam, 2014). Figure 4-1 shows the basic rectifier topologies with PFC.

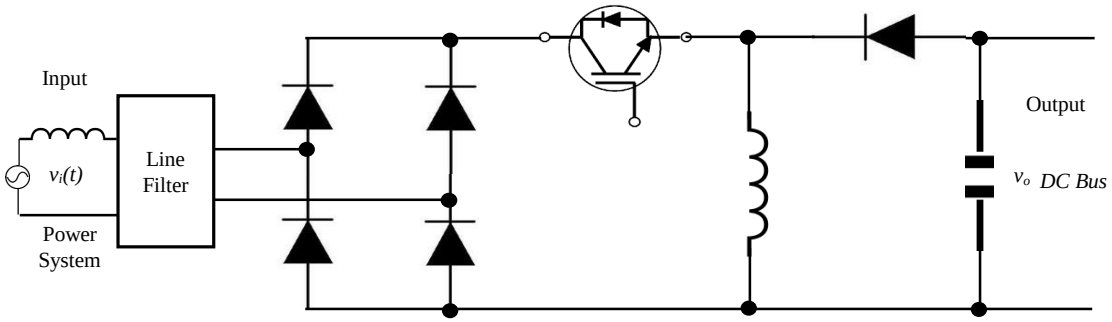
Although all the topologies of single-phase active rectifiers shown in Figure 4-1 can achieve high performance PFC, only Figure 4-1(*d*) can provide bi-directional power flow for a single-phase system.



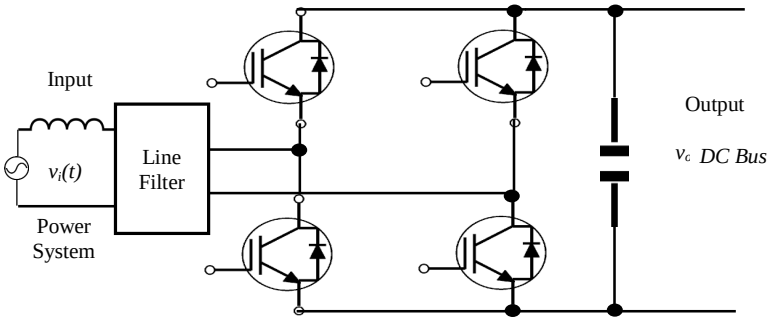
(a) Boost rectifier with PFC



(b) Buck rectifier with PFC



(c) Buck-boost rectifier with PFC



(d) H-bridge rectifier with PFC

Figure 4- 1 Basic rectifier topologies with PFC

Because the voltage stress of each switching device is only half of the total output voltage, the topology of the Vienna rectifier shown in Figure 4-2 is the most attractive (Shaon & Salam, 2014) in the application of large power rectifiers.

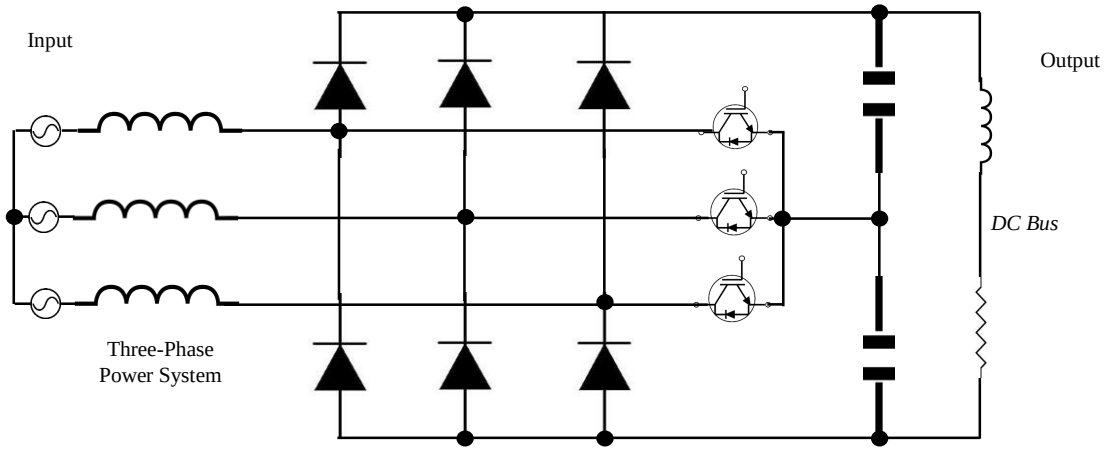


Figure 4- 2 Topology of Vienna rectifier

In terms of control measures, there are many control techniques presented in literature; examples include PWM, sinusoidal PWM (SPWM), Hysteresis PWM (HPWM), SVPWM, and Fuzzy PWM (FPWM). Although the switching losses of the SPWM can be reduced by means of modifying the carrier signal, it results in greater harmonic distortion, which causes poor power factor (Ting, et al., 2015). The control algorithm of HPWM is simple and has greater dynamic response than the PWM and SVPWM because the PWM ratio is adjusted at each PWM period; on the other hand, it has a higher ripple current (Ting, et al., 2015). The SVPWM has low switching losses and provides superior overall performance and power conversion efficiency (Ahmed & Ali, 2013), and is broadly used to implement active controllable rectifiers with PFC in three-phase systems.

The PWM algorithm is widely used in single-phase, buck, boost, and buck-boost rectifiers, according to the linear relationship between the instantaneous input and output to regulate the ratio of PWM duty.

This chapter presents a SVPWM rectifier algorithm based on three-phase GCI topology to achieve an active rectifier with PFC and presents a novel rectifier algorithm for a single-phase rectifier with PFC, so that an inverter cannot only deliver quantitative active power with quantitative RPC to the grid when it operates as an inverter, but can also implement an active rectifier with PFC.

In the topology of a three-phase inverter shown in Figure 4-3, each of the IGBTs shunts a freewheeling diode in the full-bridge inverter circuit so as to provide a complete circuit loop to protect the IGBTs from being damaged by the reverse current of an inductive load when the IGBTs are switched off. This means the circuit actually can be operated as a conventional uncontrolled rectifier while the voltage source is considered as an electrical load.

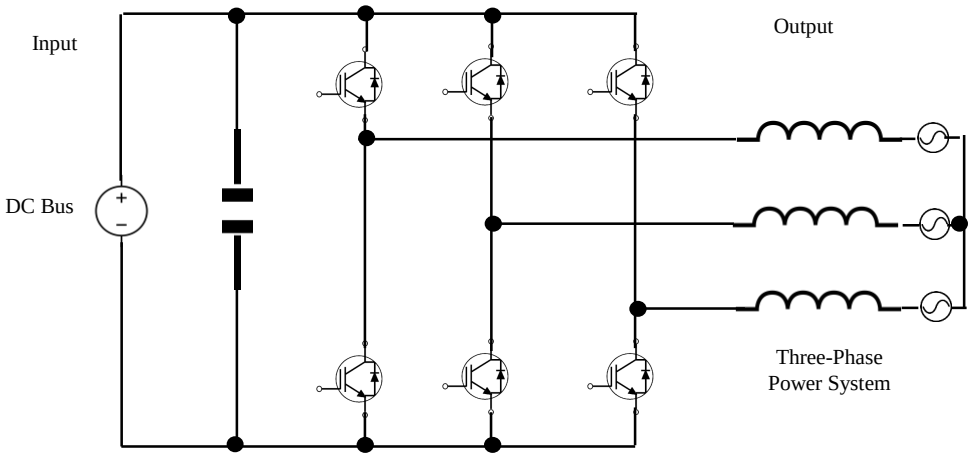


Figure 4- 3 Topology of three-phase full-bridge inverter

The disadvantages of a conventional power rectifier utilising passive diodes and capacitors contain AC current distortion and harmonic injection to the power grid. Harmonics are a major factor in determining power quality due to increasing non-linear loads; its impedance changes with the applied voltage in power systems. Harmonics cause problems in power systems and in consumer products, such as voltage distortion at the PCC (Bakar, 2008), capacitors in

equipment overheating, motor vibration, excessive neutral currents and lower power factor (Kale & Ozdemir, 2005), contribute low power conversion efficiency to the system. So improving the power factor, stabilising the rectifier DC output and reducing harmonic distortion has attracted the interest of many researchers (Moungkhum & Subsingha, 2013). Figure 4-3 is similar to Figure 2-1, they can attain bi-directional current flowing high power quality active rectifier or GCI in a three-phase system. Therefore, the following research about three-phase active rectifier is based on this concept.

4.2 Mathematical model of three-phase active rectifier

Figure 4-4 illustrates a topology from a MATLAB/Simulink of a three-phase full-bridge active rectifier. The full-bridge topology also can be operated in GCI mode if PWM control signals are changed and the load R_L in Figure 4-4 is replaced with a DC voltage source, for example DC bus link.

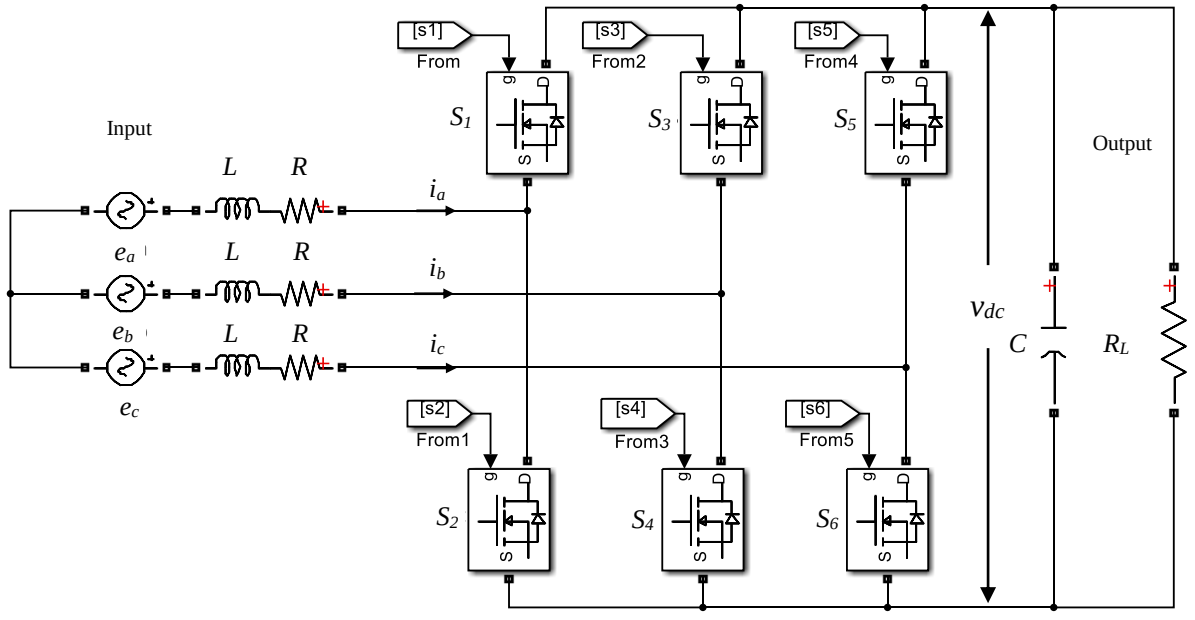


Figure 4- 4 Topology of three-phase full-bridge active rectifier

Hence, the topology illustrated above is able to implement power flowing bi-directionally. The relationships in a dynamic three-phase system of current and voltage can be described in a switched functional mathematical model as follows:

$$\begin{cases} L\dfrac{di_a}{dt} = e_a - Ri_a - v_{dc}\left(\dfrac{2S_u - S_v - S_w}{3}\right) \\ L\dfrac{di_b}{dt} = e_b - Ri_b - v_{dc}\left(\dfrac{2S_v - S_u - S_w}{3}\right) \\ L\dfrac{di_c}{dt} = e_c - Ri_c - v_{dc}\left(\dfrac{2S_w - S_u - S_v}{3}\right) \end{cases} \quad (4-1)$$

where

i_a, i_b and i_c are the instantaneous AC currents of phases *A*, *B* and *C* respectively.

e_a, e_b and e_c are the instantaneous voltages of the power grid.

v_{dc} is the voltage of the DC bus.

R is the equivalent resistance of the input filter inductors shown in Figure 4-4.

L is the inductance of the input filter inductors shown in Figure 4-4.

S_u, S_v and S_w are the switching status of the upper switching devices of each pair switching devices such as S_1 and S_2, S_3 and S_4, S_5 and S_6 in Figure 4-4 respectively, in which, logic 1 represents that the upper devices are switched on and logic 0 means switched off.

The mathematical model of the three-phase static system is clearly described by Equation (4-1). However, according to Equation (4-1) the design of the control system is a difficult challenge due to the fact that the equation shows the system is a time-variant AC system and the variables to be controlled couple each other making the system complex. Therefore, applying Clarke's and Park's transformation simplifies the process.

Through Clarke's and Park's transformation, Equation (4-1) mathematical model yields the *d-q* rotating reference frame as follows:

$$\begin{cases} L\dfrac{di_d}{dt} = e_d - Ri_d - v_{dc}S_d + \omega Li_q \\ L\dfrac{di_q}{dt} = e_q - Ri_q - v_{dc}S_q - \omega Li_d \end{cases} \qquad (4-2)$$

where

e_d and e_q are d and q components of the grid three-phase voltage vector (e_{dq}) respectively.

$v_{dc}S_d$ and $v_{dc}S_q$ are d and q components of the voltage vector of the rectifier at the three-phase grid side respectively.

i_d and i_q are d and q components of the current vector of the rectifier at the three-phase grid side respectively.

In the *d-q* rotating reference frame, assuming the e_d component of the grid three-phase voltage vector falls in the *d*-direction, the e_q component is equal to 0. The d and q components in Equation (4-2) still couple each other, so using the feed forward decoupling control method (Milosevic, 2003) with PI control for the current in the *d-q* frame, then the d and q components of the voltage vector of the rectifier, at the three-phase grid side can be obtained as follows:

$$\begin{cases} v_d = -\left(K_{dp} + \frac{K_{di}}{S}\right)(i_{dr} - i_d) + e_d + \omega Li_q \\ v_q = -\left(K_{qp} + \frac{K_{qi}}{S}\right)(i_{qr} - i_q) + e_q - \omega Li_d \end{cases} \qquad (4-3)$$

where

K_{dp} and K_{qp} are the proportional gain of the PI compensator.

K_{di} and K_{pi} are the integrator gain of the PI compensator.

i_{dr} and i_{qr} are reference current for d and q components of the current vector.

Because at the grid side, *d*- and *q*- components of three-phase VSR, $v_d = v_{dc}S_d$ and $v_q = v_{dc}S_q$, so substituting Equation (4-3) into Equation (4-2) to eliminate terms of $e_d - v_{dc}S_d + \omega L i_q$ and $e_q - v_{dc}S_q - \omega L i_d$ respectively gives:

$$\begin{cases} L\dfrac{di_d}{dt} = -Ri_d + \left(K_{dp} + \dfrac{K_{di}}{S}\right)(i_{dr} - i_d) \\ L\dfrac{di_q}{dt} = -Ri_q + \left(K_{qp} + \dfrac{K_{qi}}{S}\right)(i_{qr} - i_q) \end{cases} \qquad (4-4)$$

4.3 Current loop design

The feed forward control as described in Equations (4-3) and (4-4) reveals that the current loop of a three-phase voltage source rectifier has been successfully achieved.

This analysis only focuses on the *d-axis* quantities of current due to the symmetry between the *d* and *q* current quantities, as Equation (4-4) suggests.

In practical applications, considering some delays from sampling to computation results, in order to enhance system performance and controlled accuracy, it is necessary to add certain delays and gain parameters into a system. The *d*-component of the current loop control diagram with the perturbation of *d*-component of the power grid is illustrated in Figure 4-5.

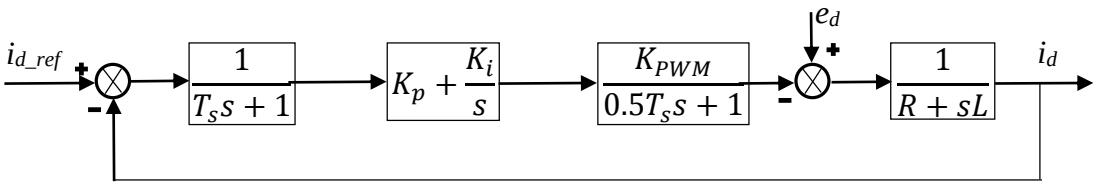


Figure 4- 5 d-component of current-loop control diagram

In Figure 4-5, T_s is the system sampling time, K_{PWM} is the system equivalent gain of the *PWM*, *R* is the equivalent resistance of the input filter inductor and *L* is the inductance, e_d is the perturbation of the voltage d-component at the grid side. In order to facilitate analysis and design of the system, writing the PI control equation in a pole-zero style (assuming the small

fluctuation of *d*-axis quantities of the grid voltage is ignored and combining the two delays in the transfer function, T_s and 0.5 T_s), then the current-loop control diagram can be simplified as in Figure 4-5.

$$K_p + \frac{K_i}{s} = K_p \frac{s + A}{s} = K_p \frac{\frac{1}{A}s + 1}{\frac{1}{A}s}$$

where $A = \frac{K_i}{K_p}$.

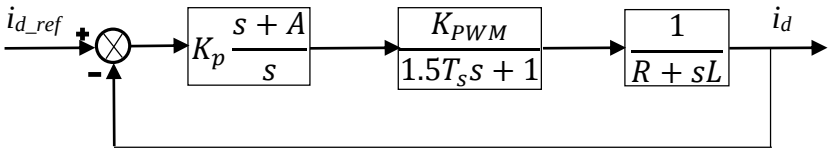


Figure 4- 6 Simplified current-loop control

According to the classical control theory, classical type I control system has faster response than type II and III. In Figure 4-6, the system could be simplified to a type I control system if PI's zero can eliminate transfer function's pole. So assuming *A = R/L*, the open-loop transfer function of the simplified current-loop control shown in Figure 4-6 can be expressed as the following mathematical model.

$$H_{id} = \frac{K_p K_{PWM}}{sL(1.5T_s s + 1)} \qquad (4-5)$$

According to Equation (4-5), the block diagram in Figure 4-6 can be equivalently further simplified as in the following figure.

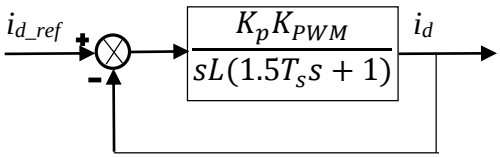


Figure 4- 7 Final d-component of current-loop control

Let $K = \frac{K_p K_{PWM}}{L}$, then the open-loop transfer function of the current i_d shown in Figure 4-6 can be expressed as:

$$H_{id} = \frac{K}{s(1.5T_s s + 1)} \qquad (4-6)$$

And the close-loop transfer function of the current i_d shown in Figure 4-7 can be obtained as:

$$E_s = \frac{\frac{K}{s(1.5T_s s + 1)}}{1 + \frac{K}{s(1.5T_s s + 1)}} = \frac{K}{s(1.5T_s s + 1) + K}$$

$$= \frac{\frac{K}{1.5T_s}}{s^2 + \frac{1}{1.5T_s} s + \frac{K}{1.5T_s}} \qquad (4-7)$$

Now convert the denominator of E_s to the standard form below

$$s^2 + 2\varsigma\omega s + \omega^2 \qquad (4-8)$$

Comparing Equation (4-7) with the standard form Equation (4-8) yields the following two quantities.

$$\omega = \sqrt{\frac{K}{1.5T_s}}$$

$$\varsigma = \frac{1}{2\sqrt{1.5KT_s}}$$

Typically the damping factor $\varsigma = \frac{1}{\sqrt{2}} \approx 0.707$ is used with $K = \frac{K_p K_{PWM}}{L}$, then the proportional parameter K_P of the current loop can be obtained as

$$K_P = \frac{L}{3T_s K_{PWM}} \qquad (4-9)$$

Because $\frac{K_i}{K_p} = \frac{R}{L}$, the integral parameter can be found

$$K_i = \frac{K_P R}{L} = \frac{R}{3T_S K_{PWM}} \quad (4-10)$$

Thus, Equations (4-9) and (4-10) represent the proportional and integral parameters of the PI controller for the current loop K_{dp} and K_{di} in Equation (4-4).

4.4 Voltage loop design

In the *d-q* rotating reference frame, the system Equation (4-8) can be expressed as

$$\begin{cases} Lpi_d = e_d - Ri_d - v_d + \omega Li_q \\ Lpi_q = e_q - Ri_q - v_q - \omega Li_d \end{cases} \quad (4-11)$$

$$v_{dc} i_{dc} = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \quad (4-12)$$

$$pv_{dc} = \frac{1}{C_o}\left(i_{dc} - i_L\right) \quad (4-13)$$

where

p is the differential operator d/dt,

e_d and e_q are the *d*-axis and *q*-axis voltage components of the power grid respectively,

R is the equivalent resistance of input filter inductor,

v_d and v_q are the *d*-axis and *q*-axis voltage components of the rectifier at the AC side, respectively,

L is the inductance of input filter inductor,

ω is the angular frequency of the voltage of the power grid in *rad/s*,

i_d and i_q are the *d*-axis and *q*-axis current components of the rectifier at the AC side, respectively,

C_o is the capacitance of the output filter of the rectifier,

i_L is the DC load current,

v_{dc} is the DC output voltage, and

i_{dc} is the rectifier output current.

Assuming the system is operating on rectifier mode with unity power factor and the *d*-axis component of the rectifier at the AC side overlaps with the *d*-axis component of the power grid (which means $e_q = 0$, $v_q=0$ and $i_q =0$), then Equations (4-11), (4-12) and (4-13) can be simplified as

$$pi_d = \frac{e_d - v_d - Ri_d}{L} \qquad (4-14)$$

$$vi_{dc} = v_d i_d \qquad (4-15)$$

$$pv = \frac{i_{dc} - i_L}{C} \qquad (4-16)$$

where,

$v = \frac{2}{3} v_{dc}$ and $C = \frac{3}{2} C_o$.

According to Equation (4-16), the second order differential equation of the output DC voltage *v* can be written as

$$v = p\left(\frac{i_{dc} - i_L}{C}\right) = \frac{1}{C} pi_{dc} - \frac{1}{C} pi_L \qquad (4-17)$$

And rearranging Equation (4-15) yields the rectifier output current i_{dc} as

$$i_{dc} = \frac{v_d}{v} i_d \qquad (4-18)$$

Differentiating both sides of the above equation gives

$$pi_{dc} = p\left(\frac{v_d}{v} i_d\right) = i_d p \frac{v_d}{v} + \frac{v_d}{v} p i_d \qquad (4-19)$$

Combining Equations (4-16) and (4-18) yields the *d*-component of the current of the rectifier at the AC side, i_d.

$$i_d = \frac{v}{v_d} i_{dc} = \frac{v}{v_d}(Cpv + i_L) \qquad (4-20)$$

Substituting Equation (4-20) into Equation (4-14) with i_d yields

$$pi_d = \frac{e_d - v_d}{L} - \frac{R}{L} \cdot \frac{v}{v_d}(Cpv + i_L) \qquad (4-21)$$

Substituting Equations (4-20) and (4-21) into Equation (4-19) with i_d and pi_d, then substituting the new Equation (4-19) into Equation (4-17) with pi_{dc} yields the second order differential equation of the DC output voltage *v* as

$$v = p\left(\frac{i_{dc} - i_L}{C}\right)$$

$$= \left[\frac{v}{v_d} p\left(\frac{v_d}{v}\right) - \frac{R}{L}\right] + \frac{v_d(e_d - v_d)}{vLC} - \frac{i_L}{C}\left[p + \frac{R}{L} - \frac{v}{v_d} p\left(\frac{v_d}{v}\right)\right] \qquad (4-22)$$

Rearranging Equations (4-22) and (4-16) as a state equation gives

$$p[X] = \mathrm{AX} + \mathrm{BU} \qquad (4-23)$$

where

$$\mathrm{X} = \begin{bmatrix} V \\ \frac{i_{dc} - i_L}{C} \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & 1 \\ 0 & \frac{v}{v_d} p\left(\frac{v_d}{v}\right) - \frac{R}{L} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{v_d(e_d - v_d)}{vLC} - \frac{i_L}{C}\left[p + \frac{R}{L} - \frac{v}{v_d} p\left(\frac{v_d}{v}\right)\right] \end{bmatrix}^0$$

Equation (4-23) is a nonlinear system due to the term $\frac{v}{v_d} p(\frac{v_d}{v})$, which results in an extremely complicated control system. In order to simplify the system, assume there is a linear relationship between the DC output voltage and the *d*-component of the rectifier input voltage at the AC side as $v_d = kv$, hence Equation (4-23) can be written as a linear system thus:

$$p[X] = \mathrm{A'X} + \mathrm{B'\ U} \qquad (4-24)$$

where

$$A' = \begin{bmatrix} 0 & 1 \\ -\frac{k^2}{LC} & -\frac{R}{L} \end{bmatrix}$$

$$B' = \begin{bmatrix} \frac{ke_d}{LC} - \frac{i_L}{C}(p + \frac{R}{L}) \end{bmatrix}^0$$

The transfer function of the close-loop control system can be found by comparing the characteristic equation of a control system with Equation (4-24), which is the state-space in controllable canonical form.

Because

$$sI - A' = \begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} - \begin{bmatrix} 0 & 1 \\ -\frac{k^2}{LC} & -\frac{R}{L} \end{bmatrix}$$

$$= \begin{bmatrix} s & -1 \\ \frac{k^2}{LC} & s + \frac{R}{L} \end{bmatrix}$$

Hence, the characteristic equation can be expressed as

$$det(sI - A') = s\left(s + \frac{R}{L}\right) + \frac{k^2}{LC} = 0$$

or

$$s^2 + \frac{R}{L}s + \frac{k^2}{LC} = 0 \qquad (4-25)$$

Then the un-damped natural frequency and damping factor can be obtained as

$$\omega = \frac{k}{\sqrt{LC}} \qquad (4-26)$$

$$\varsigma = \frac{R}{2k}\sqrt{\frac{C}{L}} \qquad (4-27)$$

A desirable value of the damping factor is between 0.6 to 0.8 with the ideal value being $\frac{1}{\sqrt{2}}$. Because, if the damping factor is too small, this will result in system oscillation; and if the damping factor is too large, the system response will be slow.

The proportional gain parameter, *k*, of the system can be selected by the appropriate choice of the input filter inductor and output filter capacitor values.

4.5 Simulation of a three-phase SVPWM active rectifier

The mathematical model of the current and voltage control loops of a three-phase power system have been designed in the previous analysis. However, accurately determining the position in a rotation frame system by sampling the voltage of the three-phase power grid is a crucial point for the field orientated SVPWM control algorithm. The SVPWM algorithm is generally composed of the following subsystems: PLL for synchronisation, Identify Sector, Firing time of the six switch devices, Park's, Clarke's, Inverse Park's and Inverse Clarke's transformations.

Detailed design of a PLL for synchronisation has been introduced in Chapter 3, and will not be described again here.

4.5.1 Identify sector

Figure 4-8 shows the relationship of the normalised sinusoidal waves of a three-phase system. The period of the sinusoidal waves of a three-phase system can be divided into 6 sectors, delimited by the zero crossing points of the 3 sine waves, i.e. 0, π/3, 2π/3, π, 4π/3, 5π/3 and 2π radians.

In Figure 4-8, the blue, green and red lines indicate the phase voltages of the A Phase, B Phase and C Phase respectively, in a three-phase balance system. Figure 4-8 shows the voltage of Phase A is greater than or equal to zero from 0 to π radians and is less than or equal to zero from π to 2π radians. Similarly Phase B is positive or zero from 0 to π/3 and from 4π/3 to 2π radians, and negative or zero from π/3 to 4π/3 radians. Also, Phase C is positive or zero from 2π/3 to 5π/3 radians, negative or zero from 0 to 2π/3 and from 5π/3 to 2π radians.

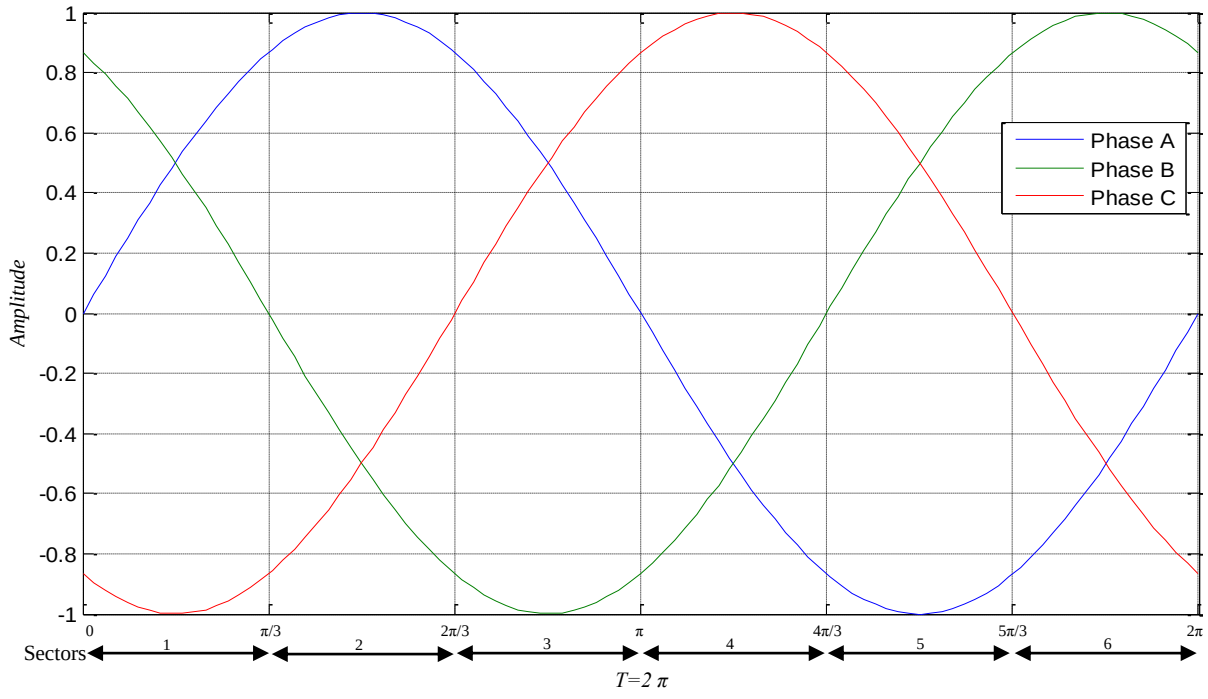


Figure 4- 8 Normalised sinusoidal waves of three-phase voltage

The sectors in Figure 4-8 can be represented logically, assuming logic 1 represents the corresponding phase voltage is greater than 0 and logic 0 represents it when less than 0, then according to the above analysis the logic relationship between the three phases in the six sectors is shown in the following table.

Sectors in Figure 4-8	**Areas**	**Phase A**	**Phase B**	**Phase C**
1	0 - π/3	1	1	0
2	π/3 - 2π/3	1	0	0
3	2π/3 - π	1	0	1
4	π - 4π/3	0	0	1
5	4π/3 - 5π/3	0	1	1
6	5π/3 - 2π	0	1	0

Table 4- 1 Logical relationship between voltage and each phase

4.5.2 Determine firing time for switching devices

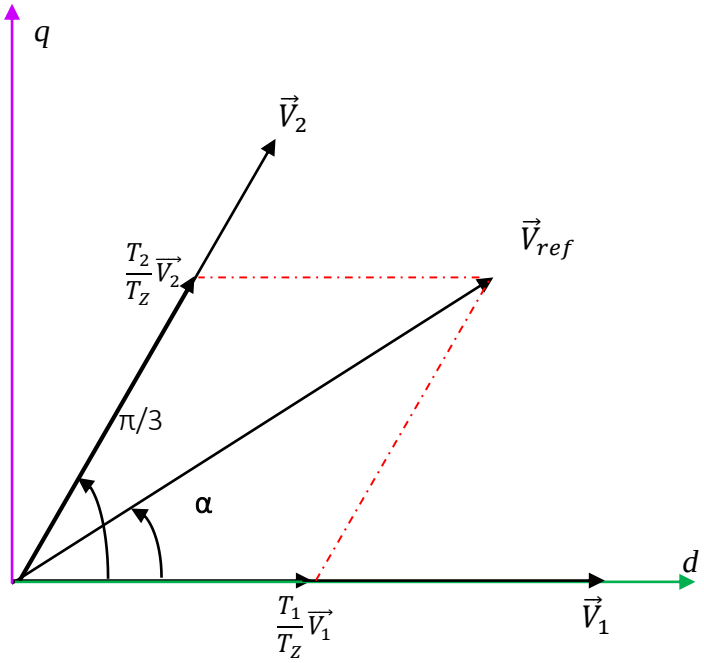


Figure 4- 9 Vector synthesis schematic in sector 1

Figure 4-9 illustrates the vector synthesis schematic in Sector 1 between 0 and π/3 radian in Figure 4-8. Assuming T_z is the normalised time unit, analysis of the figure shows that the firing times T_1 and T_2 can be obtained by the following equations:

$$\frac{|\vec{V}_{ref}|}{sin\left(\frac{2\pi}{3}\right)} = \frac{|\vec{V_1}|T_1}{sin(\frac{\pi}{3} - \alpha)} \qquad (4-28)$$

$$\frac{|\vec{V}_{ref}|}{sin\left(\frac{2\pi}{3}\right)} = \frac{|\vec{V_2}|T_2}{sin(\alpha)} \qquad (4-29)$$

Because

$$|\vec{V_1}| = |\vec{V_2}| = |U_{dc}|$$

Therefore

$$T_1 = \frac{|\vec{V}_{ref}|}{|\vec{V_1}|}\frac{sin(\frac{\pi}{3} - \alpha)}{sin\left(\frac{2\pi}{3}\right)} = M\, sin\left(\frac{\pi}{3} - \alpha\right) \qquad (4-30)$$

$$T_2 = \frac{|\vec{V}_{ref}|}{|\vec{V_1}|}\frac{sin\,\alpha}{sin\left(\frac{2\pi}{3}\right)} = M\, sin\,\alpha \qquad (4-31)$$

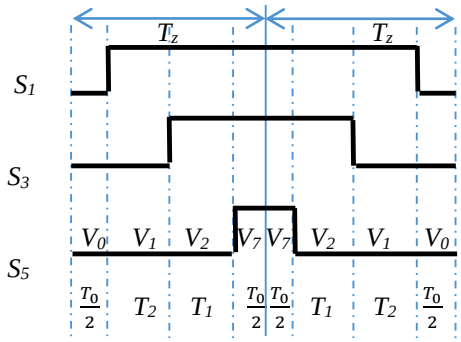
$$T_0 = T_Z - T_1 - T_2 \qquad (4-32)$$

T_0 is the time when both the upper and lower arms in the inverter-bridge are switched off, and

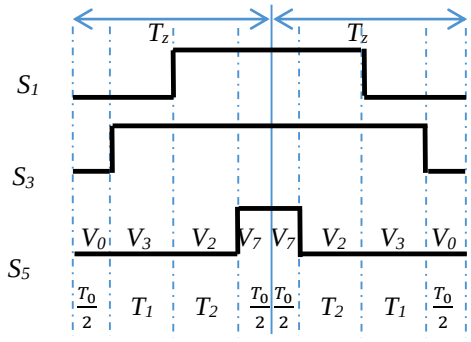
where M is the ratio of modulation,

$$M = \frac{2}{\sqrt{3}}\frac{|\vec{V}_{ref}|}{|U_{dc}|} \qquad (4-33)$$

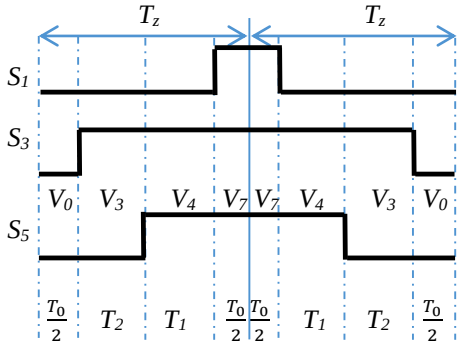
Figure 4-10 shows that one period of the output voltage is divided into 6 patterns. The patterns show the switched on/off state of the upper arms in the inverter-bridge, which is generally composed with IGBTs or MOSFETs. Because the states of lower arms are opposite to the upper arms, the state of on/off states for the lower arms are easy to obtain, therefore only the upper arm control signals are shown in Figure 4-10.



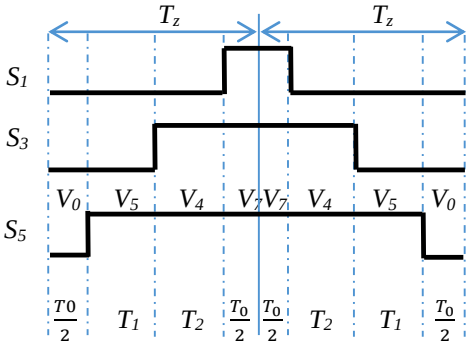
(a) Sector 1 switching state



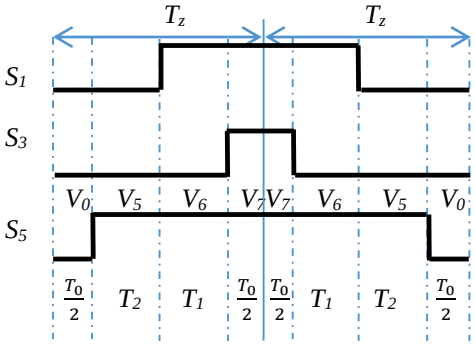
(b) Sector 2 switching state



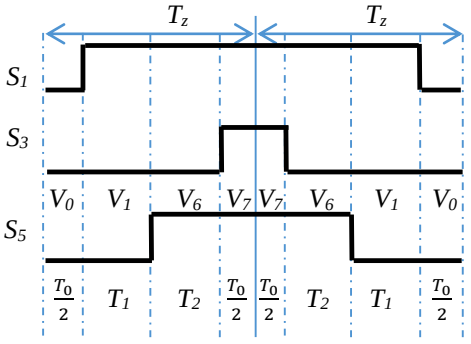
(c) Sector 3 switching state



(d) Sector 4 switching state



(e) Sector 5 switching state



(f) Sector 6 switching state

Figure 4- 10 The patterns of voltage vectors

Taken from (Cai, 2006)

The firing times of each switch in the upper arms of the bridge in the different Sectors can be obtained from Figure 4-10 as follows (Fan, 2012).

Sector 1:

$$\begin{cases} F_{S_1} = T_1 + T_2 + \frac{T_0}{2} \\ F_{S_3} = T_2 + \frac{T_0}{2} \\ F_{S_5} = \frac{T_0}{2} \end{cases} \quad (4-34)$$

Sector 2:

$$\begin{cases} F_{S_1} = T_1 + \frac{T_0}{2} \\ F_{S_3} = T_1 + T_2 + \frac{T_0}{2} \\ F_{S_5} = \frac{T_0}{2} \end{cases} \quad (4-35)$$

Sector 3:

$$\begin{cases} F_{S_1} = \frac{T_0}{2} \\ F_{S_3} = T_1 + T_2 + \frac{T_0}{2} \\ F_{S_5} = T_2 + \frac{T_0}{2} \end{cases} \quad (4-36)$$

Sector 4:

$$\begin{cases} F_{S_1} = \frac{T_0}{2} \\ F_{S_3} = T_1 + \frac{T_0}{2} \\ F_{S_5} = T_1 + T_2 + \frac{T_0}{2} \end{cases} \quad (4-37)$$

Sector 5:

$$\begin{cases} F_{S_1} = T_2 + \frac{T_0}{2} \\ F_{S_3} = \frac{T_0}{2} \\ F_{S_5} = T_1 + T_2 + \frac{T_0}{2} \end{cases} \quad (4-38)$$

Sector 6:

$$\begin{cases} F_{S_1} = T_1 + T_2 + \frac{T_0}{2} \\ F_{S_3} = \frac{T_0}{2} \\ F_{S_5} = T_1 + \frac{T_0}{2} \end{cases} \quad (4-39)$$

4.5.3 Over modulation

Generally, calculating the firing time of each of the switching devices in the inverter-bridge does not cause any problems in theory. In practical applications, however, over modulation errors can be introduced in the calculation of the vector due to following reasons:

- Mathematical operations in the algorithm (particularly multiply, divide and trigonometrical operators) may introduce rounding/truncation errors; and
- Calculation across Sector boundaries may result in errors in the synthesis of the vectors.

Therefore, in order to solve the problem of over modulation, linear modulation and non-linear modulation are employed to control over modulation (Fan, 2012).

If the module is working during the dead time, i.e. when T_0 is greater than or equal to 0, Equations (4-30), (4-31) and (4-32) will be executed. Otherwise Equations (4-40), (4-41) and (4-42) below will be executed.

$$T_1{}' = \frac{T_1}{T_1 + T_2} T_z \quad (4-40)$$

$$T_2{}' = \frac{T_2}{T_1 + T_2} T_z \quad (4-41)$$

$$T_0 = 0 \qquad (4-42)$$

4.5.4 Generating controlled PWM for SVPWM

Figure 4-11 illustrates the principle of PWM generation. A triangular waveform carrier wave is compared with a sine wave reference signal, the state of output is positive when the value of the reference signal is greater than the carrier waveform, otherwise it is negative.

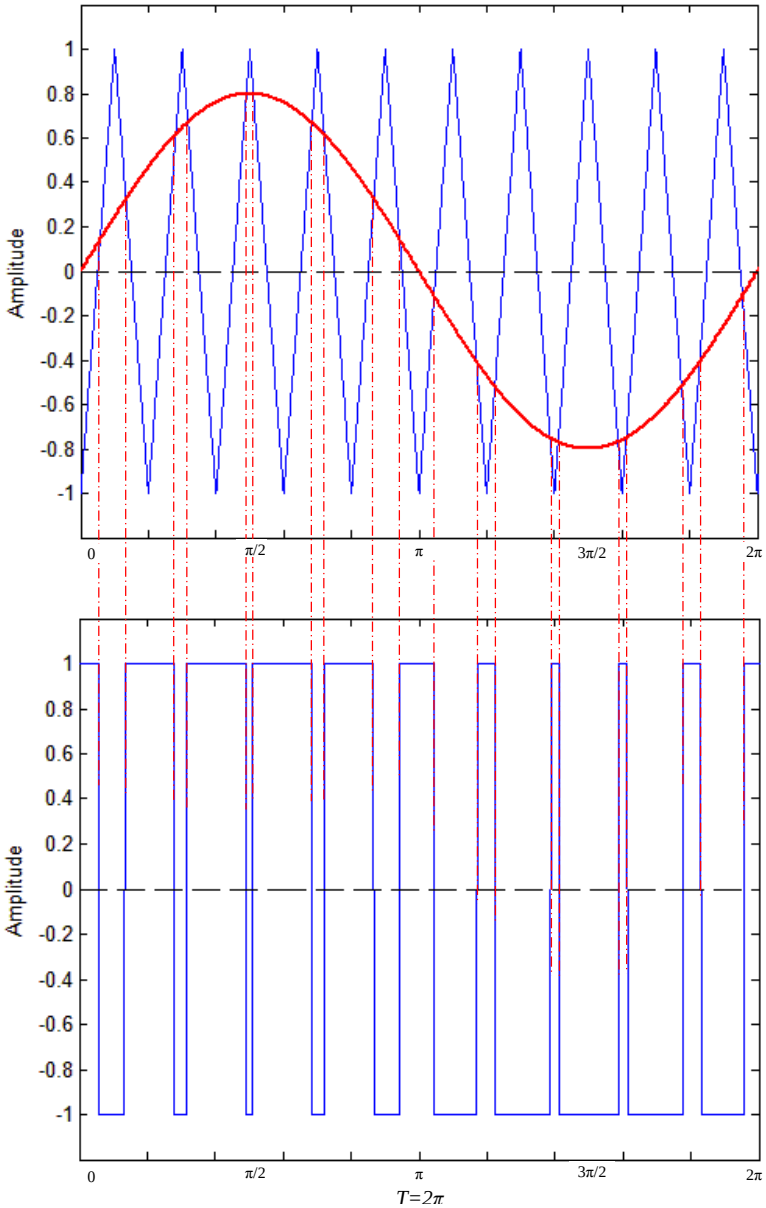


Figure 4- 11 The principle of PWM generation

The output logical relationships of PWM can be described in mathematical form as follows:

$$V_{PWM} = \begin{cases} 1 & if\ V_{ref} \geq V_{tri} \\ -1 & otherwise \end{cases} \qquad (4-43)$$

where

V_{PWM} is the logical value of PWM output, 1 represents upper arm is switched on, -1 represents lower arm is switched on

V_{ref} is the refrence modulation sine wave

V_{tri} is the triangular carried wave

In Figure 4-11, the modulation waveform is a refrence sine wave, but for SVPWM algorithm, the ideal modulation waveforms is a saddle-like shapes, as in Figure 4-12. To compare with tranditional sine modulation waveform, the utilization of the DC-bus voltage was improved (Infineon Technologies AG, 2006).

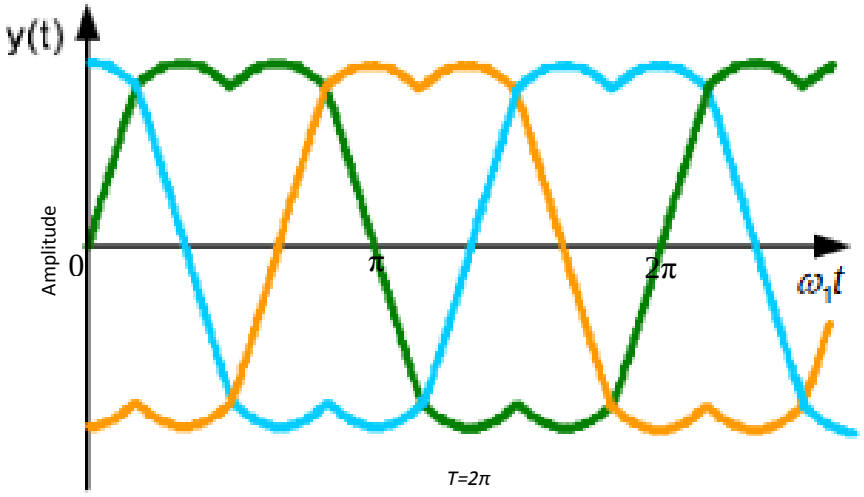


Figure 4- 12 Ideal modulation waveform of SVPWM

4.6 Modelling three-phase SVPWM rectifier

All the models of Clarke, Inverse Clarke, Park, Inverse Park, Identify Area and Firing time have been modelled as MATLAB Function Blocks as this is the most convenient way to

achieve the complex mathematical calculations required and to implement the design in a real time embedded system in the future. The input filter inductor coils have an inductance of 3mH and equivalent resistance of 0.5Ω. The sample time of system is 100ms. The frequency of the power grid is 50Hz.

4.6.1 Modelling identify area and firing time

Figure 4-13 illustrates the modelling of current controlled-loop according to Equation (4-3) stated previously, and the parameters of the PI controller are listed in the figure.

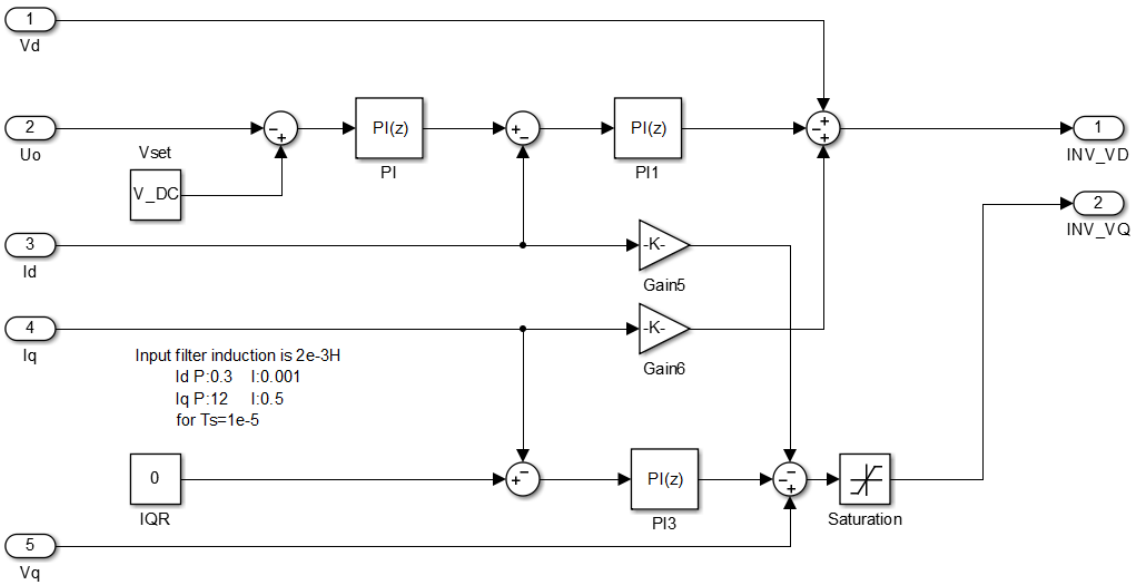


Figure 4- 13 Modelling of current controlled-loop

Figure 4-14 depicts a model of the three-phase SVPWM rectifier, which can be operated as a normal SVPWM rectifier without PFC, or a SVPWM rectifier with PFC which requires a change of the PWM control signals for the Rectifier Bridge, i.e. the block of SVPWM, which generates PWM signals for normal rectifier without PFC to be changed as the block of PFC SVPWM, which generates PWM signals for rectifier with PFC. The blocks of V_CLARKER and I_CLARKER transform three-phase reference frame into stationary orthogonal reference frame for voltage and current of the grid respectively. The blocks of V_PARK and I_PARK

convert vectors in two-phase stationary orthogonal frame into rotating orthogonal reference frame for voltage and current respectively. The block of Synthesised Vd_Vq implements Equation (4-7), the block of INV_PARK achieves inverse of Park's transformation from the rotating orthogonal reference frame to the stationary orthogonal frame.

In the simulation, the peak value of the input three-phase AC voltage is 310V and the frequency is 50Hz; the input filter is formed by an inductor 3mH and an equivalent resistor 0.5Ω in serial, the capacitance of the output filter capacitor is 2000μF, the resistance of the load is 30Ω and the sampling time of simulation system is 10μs.

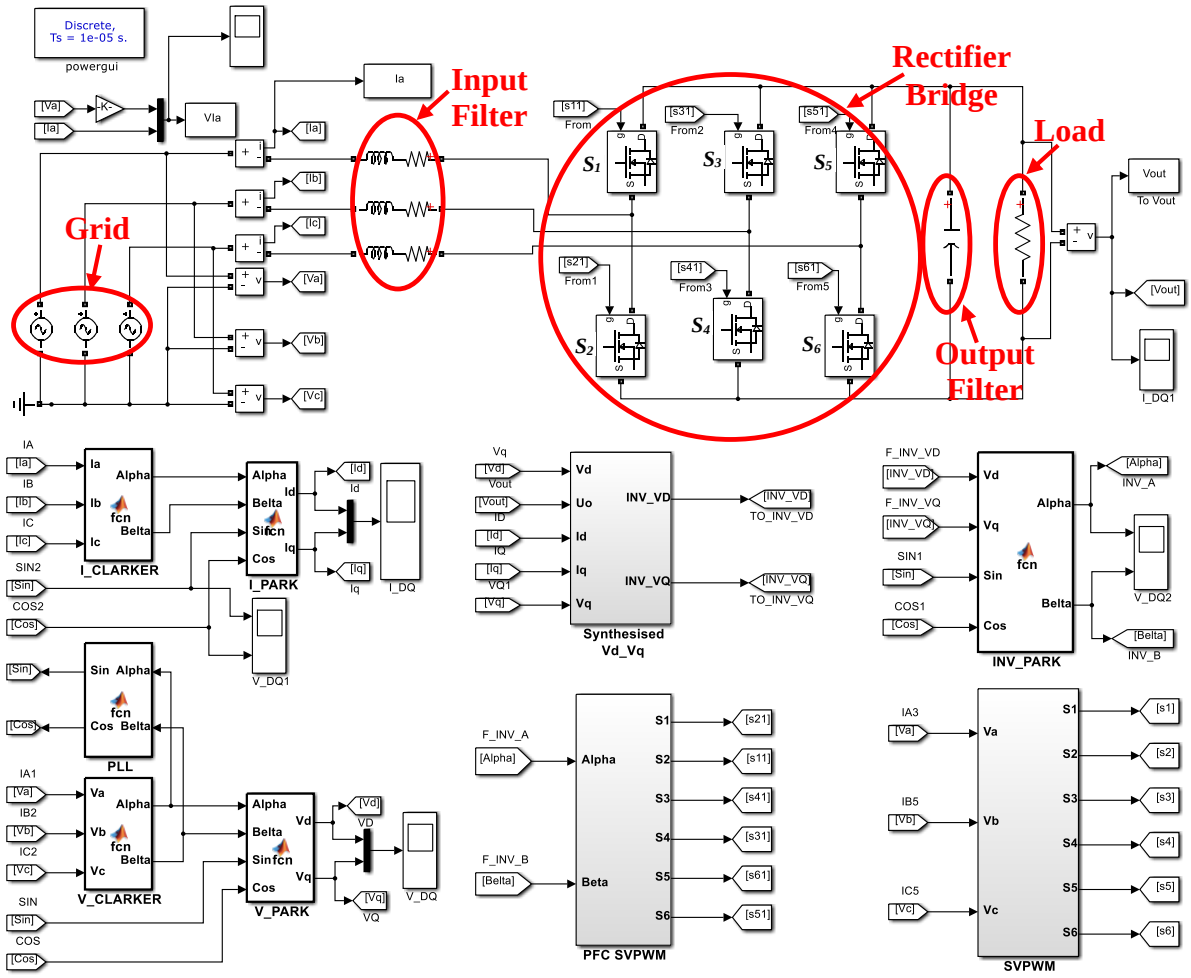


Figure 4- 14 Modelling of three-phase SVPWM rectifier with/without PFC

As the figure shows, the topology of the rectifier bridge is composed of six IGBT devices, which is exactly the same as the inverter-bridge of a three-phase GCI.

For GCIS, if the Load in the figure is considered as a DC voltage source or DC bus then the system can be operated as GCI injecting power into the power grid.

Figure 4-15 shows the simulated results of the generated normalised control saddled waves of the SVPWM which are compared with counters to generate the PWM control signals. The experimental results of control saddled waves are shown in Figure 4-16, 4-17 and 4-18 which are used to compare with the up-down timer register in the DSP chip to generate PWM signals to control switched devices S_1 – S_6. The saddled waves in Figure 4-16, 4-17 and 4-18 were captured through CCS 3.3 IDE for TI DSP.

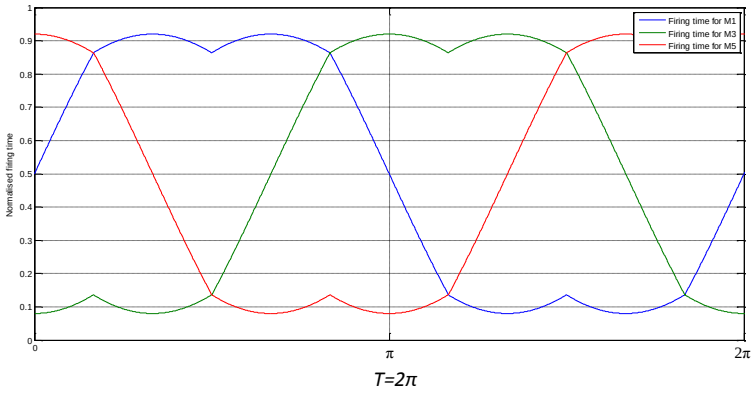


Figure 4- 15 Generated saddled modulation waveform

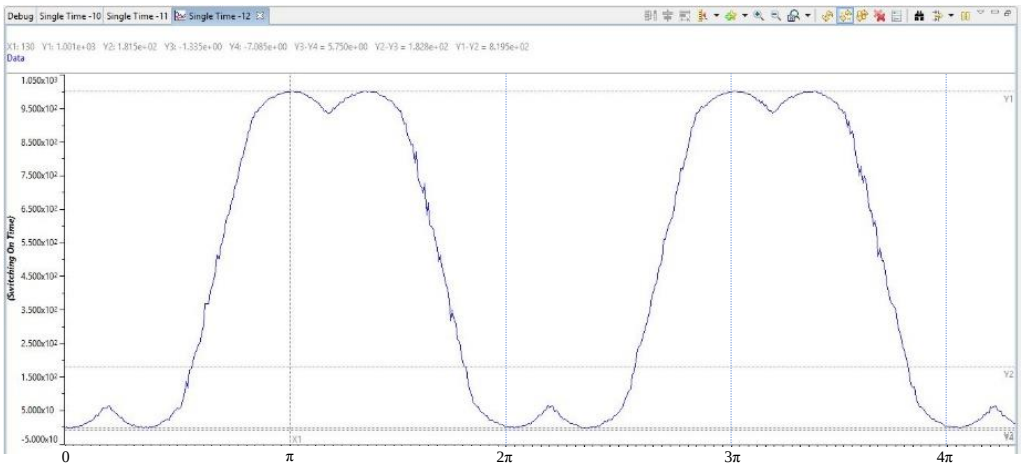


Figure 4- 16 Experiment result of Phase A saddled carried waveform

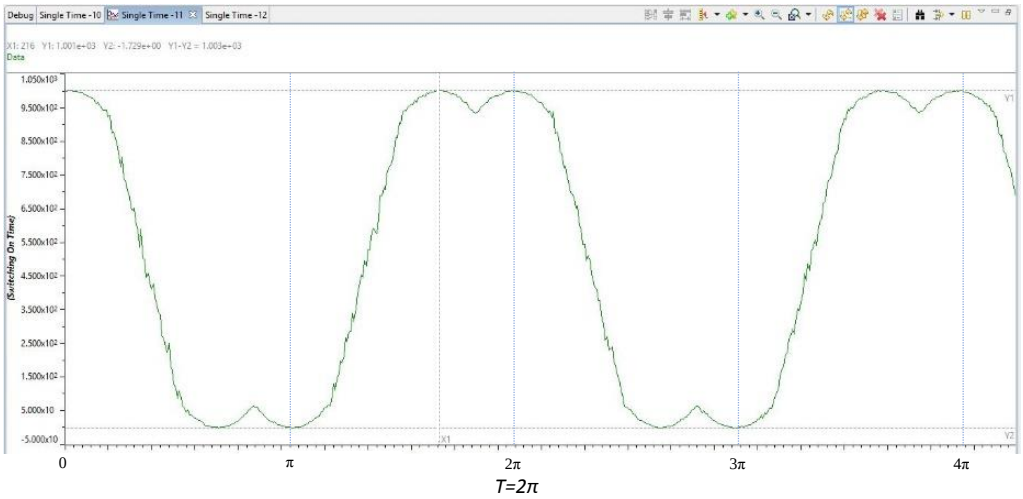


Figure 4- 17 Experiment result of Phase B saddled carried waveform

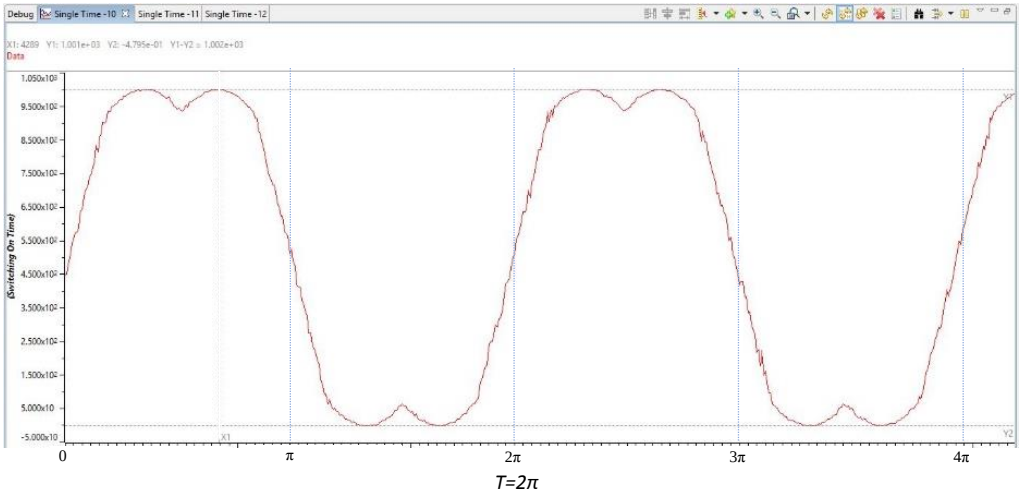


Figure 4- 18 Experiment result of Phase C saddled carried waveform

As Figure 4-19 shows, although the rectifier employs SVPWM algorithm to generate PWM control signals, there is no current control-loop for PFC. Therefore, the input current appears as a smooth sine wave, but lags the voltage due to the filter inductor coils. Figure 4-20 illustrates the results of SVPWM rectifier with PFC, in which the current is in phase with the voltage. After PFC, analysis and comparison of the current waveforms in Figure 4-21, shows the THD of the input current is 1.72%, less than the general threshold 3%, which means the quality of input current is satisfied.

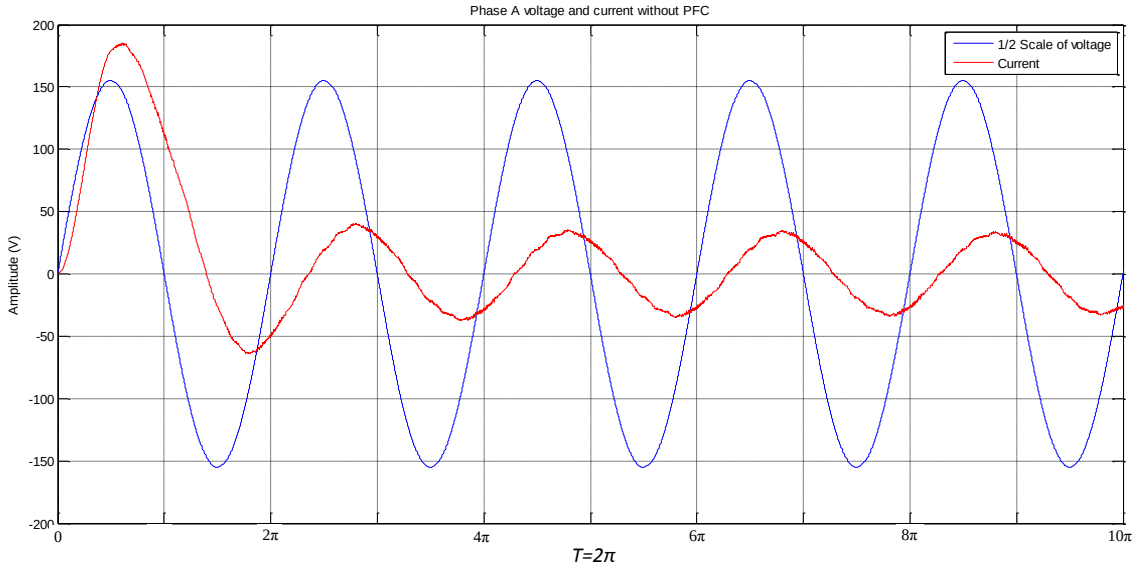


Figure 4- 19 Phase A current and voltage without PFC

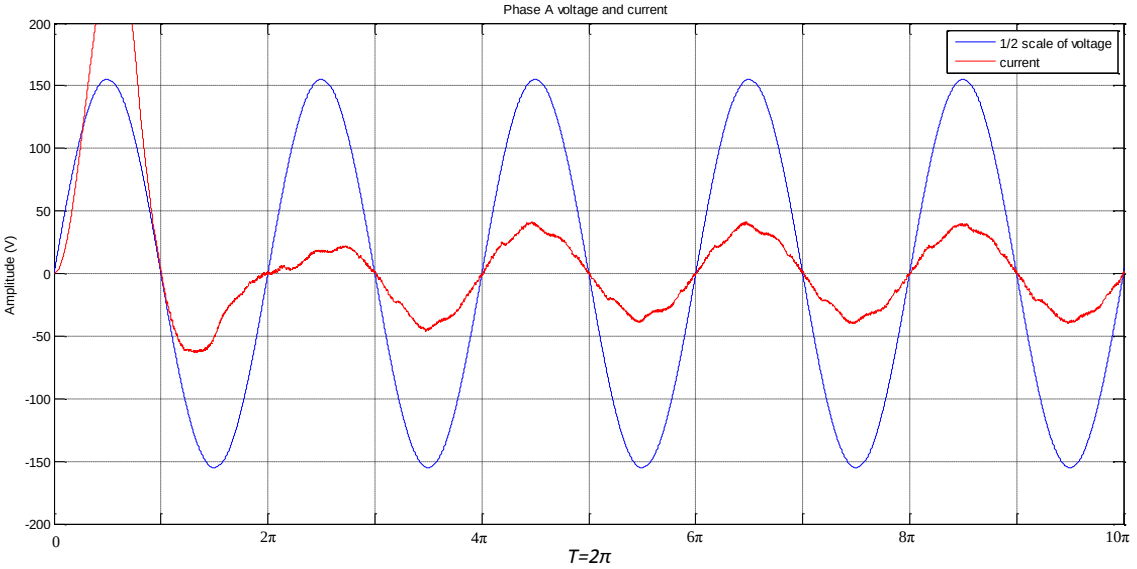


Figure 4- 20 Phase A current and voltage after PFC

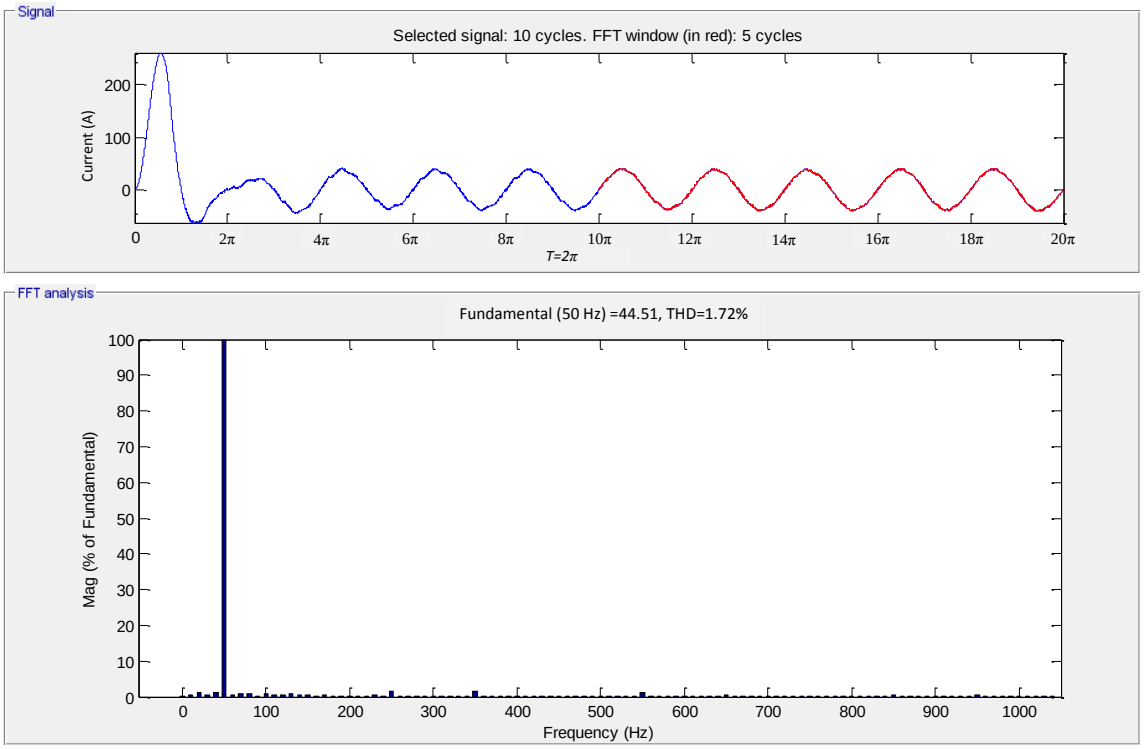
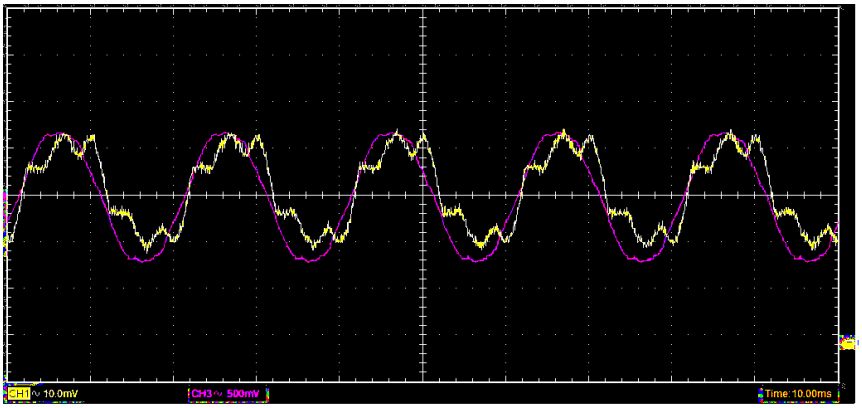
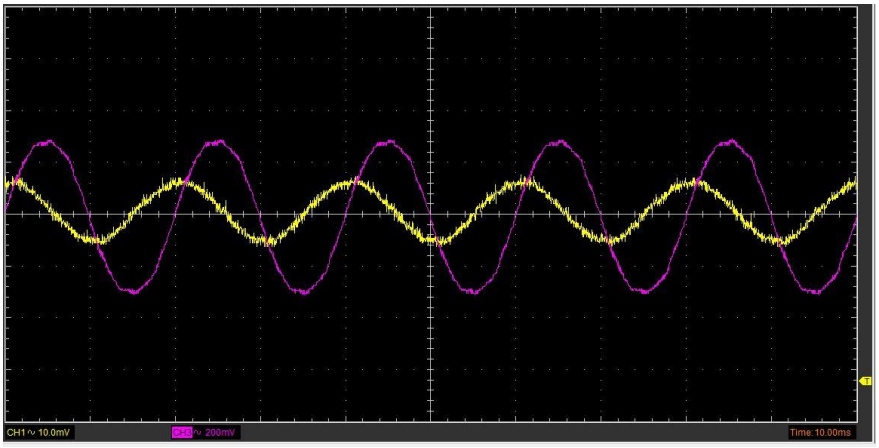


Figure 4- 21 Analysis of harmonic distortion

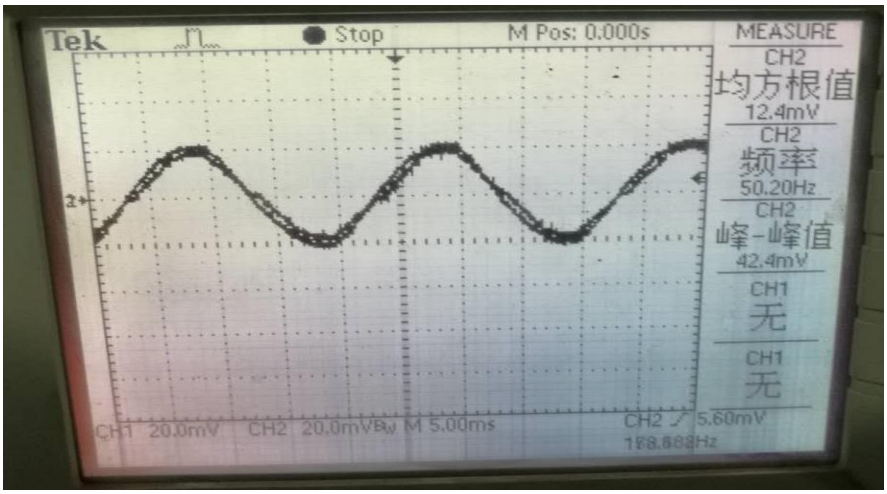
Figure 4-22 (a) illustrates the experimental comparison of Phase A current and voltage waves of an uncontrolled rectifier, in the figure, the yellow trace is voltage signal and the magenta trace is current signal. Intuitively there is gross distortion on the current wave. Figure 4-22 (b) shows experimental results of SVPWM rectifier without PFC; it can be seen that the distortion content of the input Phase A current is eliminated using the SVPWM algorithm. However, although the power quality has been dramatically improved, the power efficiency and voltage utilisation still need to be improved. Figure 4-22 (c) demonstrates the results of SVPWM rectifier with PFC, as the figure shows that the current is in phase with the voltage on Phase A when the SVPWM algorithm, including voltage and current control-loops are used.



(a) Uncontrolled rectifier voltage and current



(b) SVPWM rectifier voltage and current without PFC



(c) SVPWM rectifier voltage and current with PFC

Figure 4- 22 Experimental results

4.7 Modelling single-phase rectifier

P-Q theory is a powerful tool to apply for three-phase system (Afonso, et al., 2003). Three-phase active rectifier has been described previously and successfully modelled in section 4.6. The theory of this three-phase active rectifier is based on control of reactive current which is obtained through Clarke and Park transformations. Using the same approach, a novel method of single-phase rectification is presented in this section. The strategy of single-phase rectifier with PFC is illustrated in Figure 4-23.

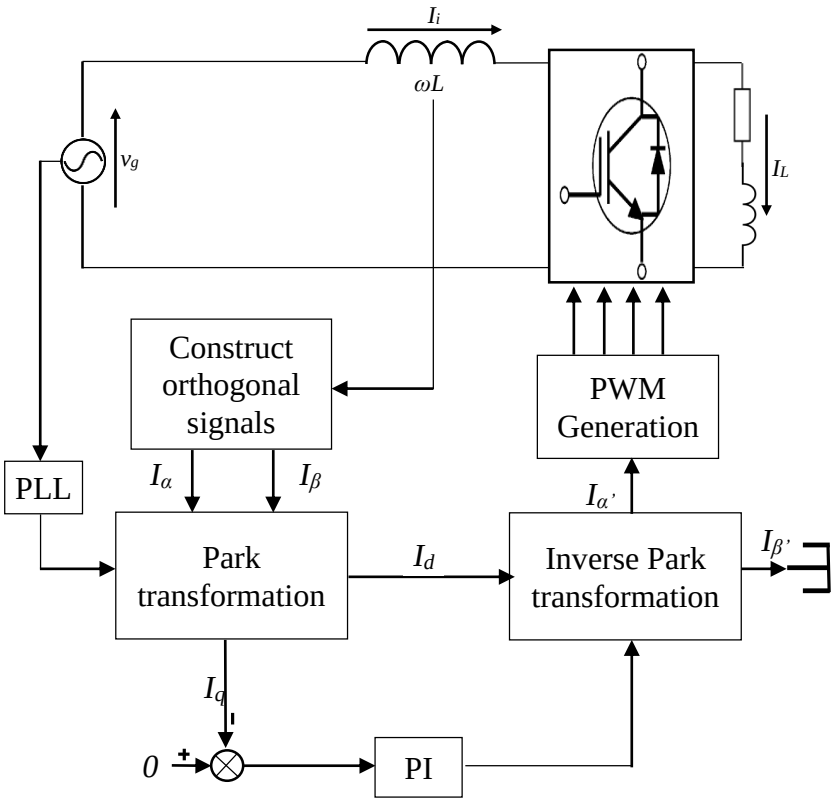


Figure 4- 23 Strategy of single--phase rectifier with PFC

For a single-phase system Clarke's and Park's three-phase transformations are not appropriate (Microsemi, 2013). Therefore, the novel approach for a single-phase rectifier presented here, constructing a new pair of orthogonal signals against with the sample of the instantaneous input current signal by the SOGI is introduced in Chapter 3. Then the Park transformation can be employed to decompose active and reactive currents, the reactive current being controlled to

be as close to zero as possible. Then using the Inverse Park's transformation to generate a reference current, which is used to compare with the actual input current to generate PWM control signals for the rectifier bridge.

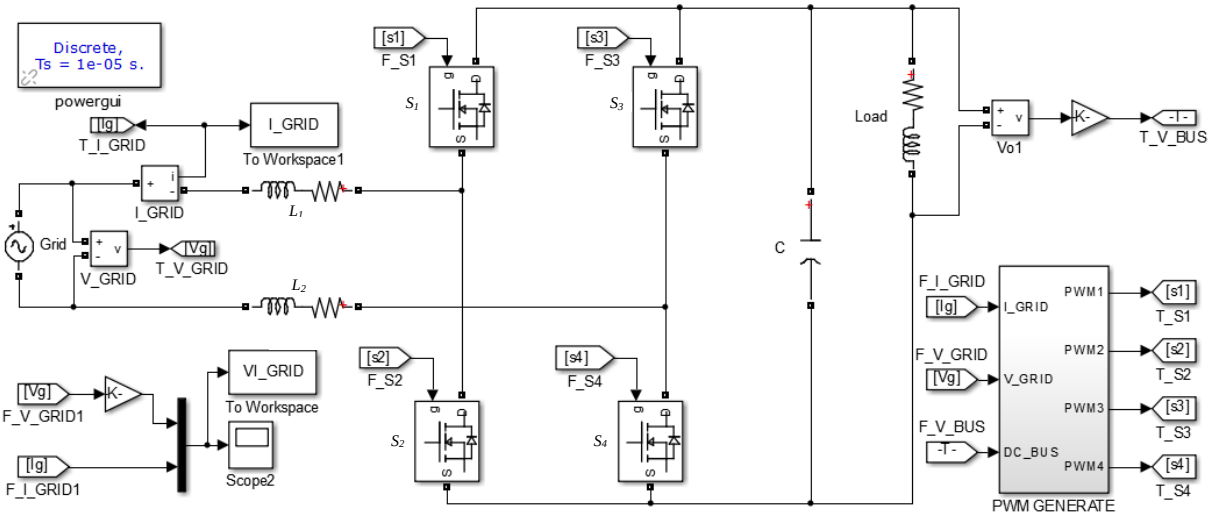


Figure 4- 24 Model of single-phase rectifier with PFC

Figure 4-24 shows the complete simulation model of the single-phase rectifier with PFC in MATLAB/Simulink environment. The sampling time of the simulation model is 10μs, the peak value of input voltage sine wave is 110V, the inductance of both input filter inductors L_1 and L_2 are 2.5mH, the load comprises a 1mH inductor in serial with a 30Ω resistor and the capacity of the output filter capacitor is 4700μF.

Figure 4-25 shows the results of the single-phase rectifier, in which the current is in phase with the voltage, and Figure 4-26 illustrates the harmonic analysis of input current. This, analysis shows less than 1.4%, THD, which means power quality of the input has been greatly improved and enhanced.

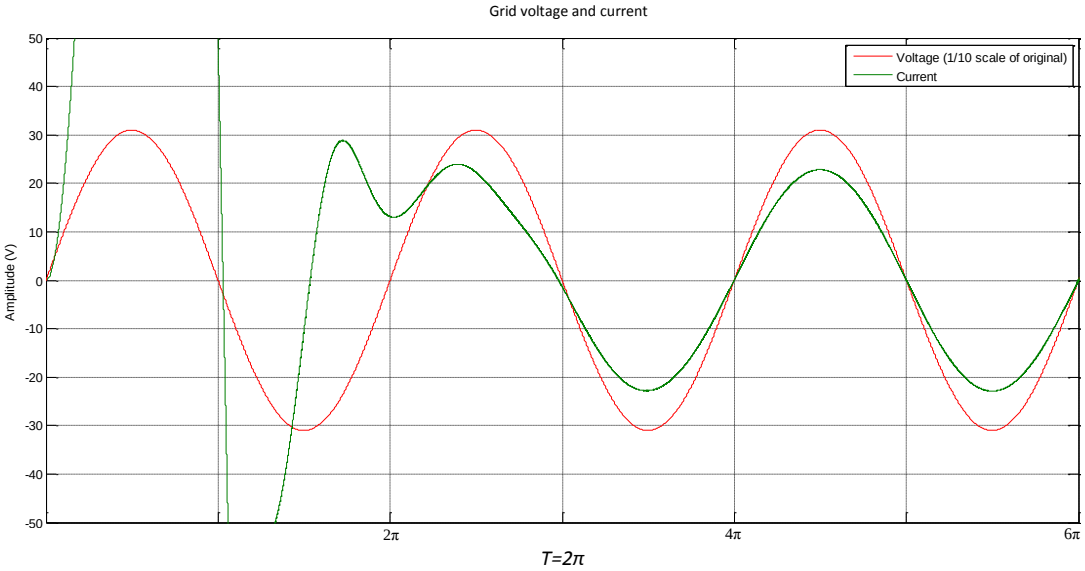


Figure 4- 25 Results of single-phase rectifier

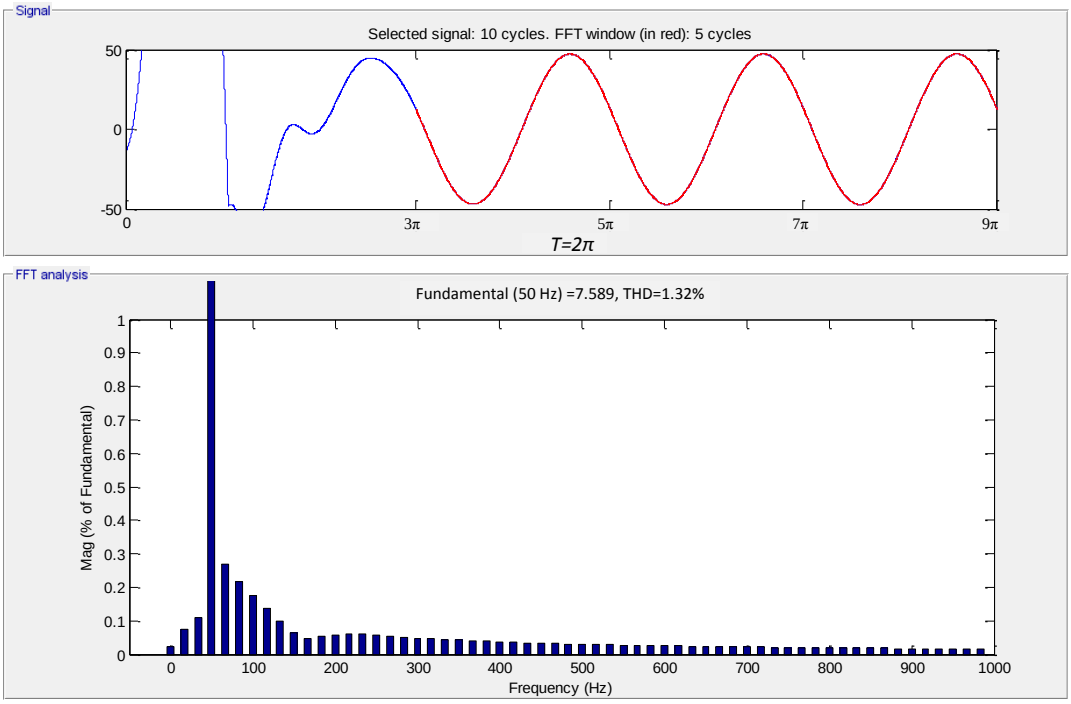


Figure 4- 26 Harmonic analysis of input current

4.8 Summary

In order to implement a DC/AC power inverter so that electrical power can be converted bi-directionally either from the AC grid side to the DC bus side or from the DC bus side to the

AC grid side, an ideal rectifier and inverter based on the same topology for both single-phase and three-phase power system have been considered in this chapter.

Using the concept of three-phase PFC rectifier and the P-Q theory of instantaneous reactive power, through a detailed mathematical analysis and design process for a three-phase SVPWM rectifier, a novel method of constructing a pair of orthogonal signals for current sampling and using Clarke's and Park's transformation to split active and reactive components of the input current for single-phase rectifier for a bi-directional H-bridge converter, was presented in this chapter.

Simulation models of both three-phase and single-phase systems were developed in MATLAB/Simulink environment. By analysing the simulation results, it is apparent that the input power quality is considerably improved.

Chapter 5 Bi-directional interleaved boost/buck DC/DC converter

5.1 Introduction

For a renewable power system, directly injecting power into the power grid impacts the grid power quality, due to renewable source intermittency and random characteristics. In order to stabilise inverter output and enhance end-user's benefits from integrated renewable power system, a battery bank is typically included at the user terminal to buffer fluctuations and meet end-user's expectations.

Battery bank capacity is proportional to cost, so the main problem in providing the best cost-effective configuration of the battery bank is that the battery bank terminal voltage might not match the DC Bus voltage. In this case, it is necessary to have a bi-directional DC/DC converter to interface between a higher DC bus potential and lower battery voltage.

This chapter presents a novel four-phase interleaved boost/buck topology to implement power flow bi-directionally between the higher and lower potentials, which means the boost and buck can be achieved on a same topology by swapping the input and output terminals.

With the rapid development of power electronics, to improve power supply quality, reliability and efficiency, there are a number of topologies for DC/DC converters that have been put forward in the past two decades. According to the method of electrical connection, the DC/DC converter is categorised into two classes: isolated and non-isolated. Normally, an isolated DC/DC converter uses a transformer between the input source and output circuit, providing electrical isolation via the magnetic coupling in the transformer. The advantage of an isolated

converter is a high safety level; however the drawback is loss of power in the transformer and associated isolation circuitry and high cost.

In this project, it was decided to simulate a non-isolated DC/DC converter because the fundamental principle of isolated and non-isolated converters are the same.

There are four basic converter topologies employed practically in renewable power systems: the step-down (Buck) circuit, the step-up (Boost) circuit, the boost-buck converter and the Ćuk converter (Maniktala, 2006).

Whatever the converter topology, it can be subdivided into continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In a CCM converter, the current through the inductor *L* is always positive and never equal to zero in any switching period of the switching device *M*; in a DCM converter, the current is not always positive.

5.2 Buck converter

A step-down circuit, also known as a buck circuit, is shown in Figure 5-1. The circuit consists of a voltage source v_s, a switching device S_1 connected in series with v_s, a reverse biased diode D_1 shunts the voltage source and switch combination, across which an LC filter provides the output to a resistive load R_1.

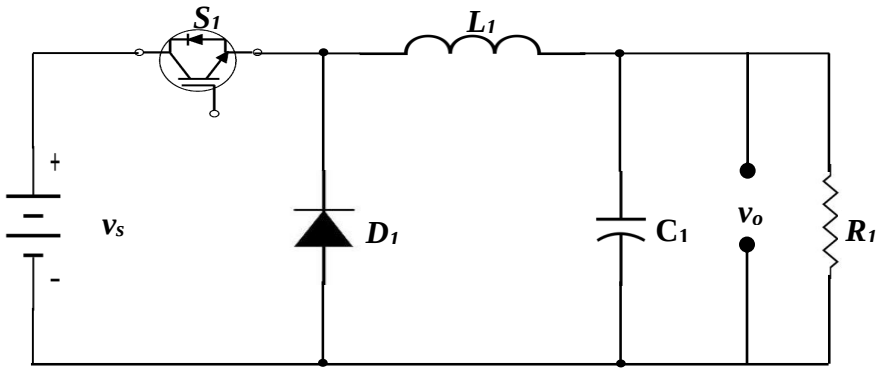


Figure 5- 1 Topology of buck converter

For the buck converter, from Figure 5-1, in the steady state, the relationship between the input voltage v_s, output voltage v_o, and the duty ratio of switching time D can be obtained as (Czarkowski, 2007):

$$(v_s - v_o)DT = v_o(1 - D)T \tag{5-1}$$

Dividing both sides by the switching time period, T, and rearranging the relationship between output and input voltage, we have:

$$A \equiv \frac{v_o}{v_s} = D \tag{5-2}$$

where A is the buck circuit gain.

For the buck circuit, based on Equation 1, it can be summarised that the input voltage is always greater than the output voltage. Therefore, this topology is appropriate for applications where the load voltage is relatively low, such as a battery charging circuit. This type of circuit is commonly used in laptop power supply.

If the switching frequency is fixed, the inductor inductance L_1 in the buck circuit determines whether the circuit operates in CCM or DCM mode. The critical inductance between CCM and DCM is given by (Czarkowski, 2007):

$$L_1 = \frac{(1-D^2)R_1}{2f} \tag{5-3}$$

L_1 is the critical inductance of the inductor,

D is the ratio duty of the switching period for switching devices S_1,

R_1 is the load resistance in Figure 5-1, and

f is the switching frequency.

If the inductance of inductor is greater than the critical inductance L_1 then the circuit operates in CCM, otherwise in DCM.

5.3 Boost converter

Figure 5-2 shows the circuit of a simple boost converter. It consists of a voltage source v_s, in series with an inductor L_1 used for energy storage, a switching device S_1, a diode D_1, a filter capacitor C_1 and a load R_1.

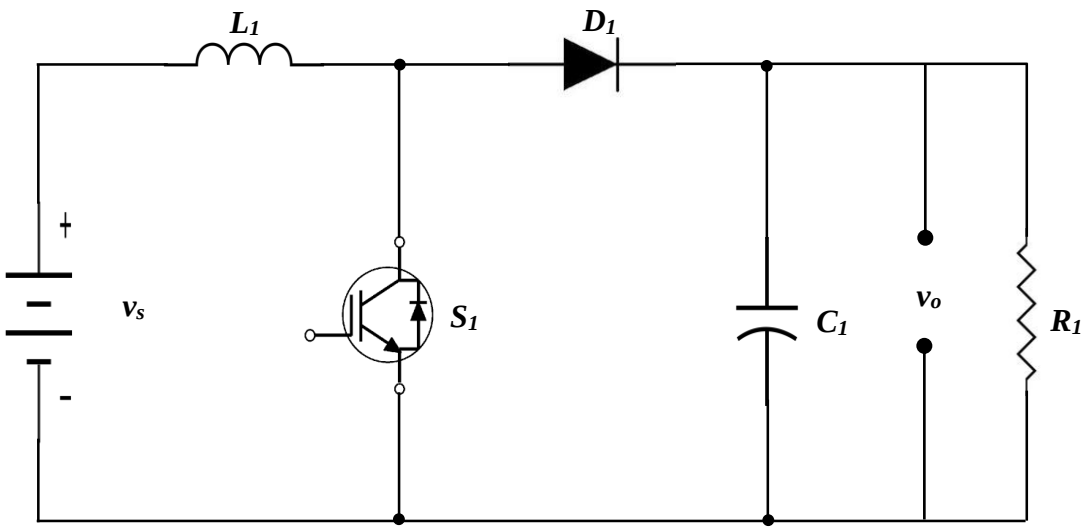


Figure 5- 2 Circuit of boost converter

When the switching device S_1 is conducting, energy is stored in the inductor L_1. Assuming all devices are ideal and the voltage across the capacitor C_1 is greater than the source voltage v_s, then the diode D_1 is reversely biased and the capacitor provides the energy needs of the load R_1. During this time, i.e. the switching device S_1 is conducting, the current through the inductor rises linearly. When the switching device S_1 is opened, the diode D_1 conducts the current through the inductor L_1, providing current for the load R_1 and (re)charging the capacitor C_1.

In the steady state, using Faraday's law, the relationship between the switching duty ratio of the switching devices D_1, the output voltage v_o and the input voltage v_s can be obtained as (Czarkowski, 2007):

$$v_s DT = (v_o - v_s)(1 - D)T \tag{5-4}$$

Dividing both sides by the switching period, *T*, and rearranging the relationship between output and input voltage, we have:

$$A \equiv \frac{v_o}{v_s} = \frac{1}{1-D} \tag{5-5}$$

where *A* is the boost circuit gain.

Equation 5-5 shows that the boost circuit gain is always greater than 1, which means that the output voltage is higher than the input voltage. Hence, the boost circuit is widely employed in the field of RES to increase the voltage of DC bus link in order to ensure that power can be adequately injected into the power grid.

For the boost circuit, once the switching frequency is confirmed, the inductance of L_1 determines the operating mode of circuit, as given by (Czarkowski, 2007):

$$L_1 = \frac{(1-D)^2 DR}{2f} \tag{5-6}$$

where

L_1 is the critical inductance of inductor in Figure 5-2,

D is the ratio duty of the switching period,

R_1 is the load resistance in Figure 5-2, and

f is the switching frequency.

If the inductance of inductor in Figure 5-2 is greater than L_1, the circuit is operated in CCM, otherwise in DCM.

Most MPPT units, which are used in the application of solar PV system, are based on DC to DC converters of either a Boost or Buck topology, and the article (Glasner & Appelbaum, 1996) demonstrates that a Boost converter has higher power conversion efficiency than a Buck converter.

All switch-mode power supplies are made up of a buck or boost topology or combination of buck and boost with or without transformers (Billings, 2003). In a buck converter the input current is discontinuous and the output current is continuous. Conversely, in a boost converter the input current is continuous and output current is discontinuous (Billings, 2003; Maniktala, 2006).

5.4 Interleaved boost circuit

Interleaved topology was introduced to overcome the problems of ripple current, thermal dissipation and large filter capacitor bank requirements at the input or output terminal of switch-mode power supplies, widely employed in the application of computer power supply.

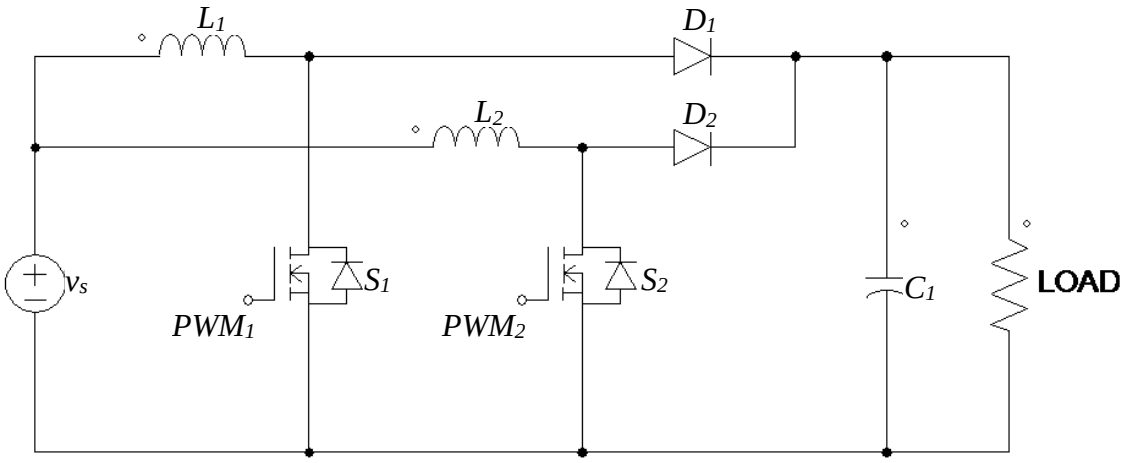


Figure 5- 3 Basic interleaved boost topology

Figure 5-3 shows a basic interleaved boost topology which consists of two boost circuits, S_1 and S_2 connected in parallel. The two PWM signals, PWM_1 and PWM_2 driving the switches

are mutually 180 degree out of phase. The total current supplied for the load is split between the two paths, reducing the required size of the inductors and capacitor and significantly reducing the I^2R losses (thermal dissipation) compared to the conventional boost topology. Also, because the total current is divided into two paths to deliver to the output terminal, the two path currents are eventually combined at the capacitor C_1 in Figure 5-3, so the ripple frequency at the load is doubled but at smaller amplitude therefore can be more easily filtered.

The interleaved topology has the following four advantages:

- improvement in the power quality;
- increased efficiency from reduced thermal dissipation in the circuit;
- reduced size of the filter inductor; and
- reduced output ripple voltage.

Typically, a renewable power system operates at a high voltage potential, and there is a potential difference between the DC bus and the battery bank. For this project, a four-phase interleaved bi-directional boost-buck converter (IBDBBC) is proposed and modelled in MATLAB/Simulink.

5.5 Modelling four-phase IBDBBC under boost mode

A four-phase IBDBBC is derived from a conventional boost and buck converter. For comparison purposes, it is essential to create both simulation models for the four-phase IBDBBC and the conventional boost converter with the same parameters for the components in both circuits. Figure 5-4 is a simulation model of a conventional boost converter which is created in MATLAB/Simulink. In the figure, the input DC voltage source v_s is 200V and the expected output voltage at the filter capacitor C_1 terminal is 450V. In the circuit, the inductance of energy stored inductor L_1 is 200μH, the inductance of output filter inductor L_2 is 50μH, the capacitance of output filter capacitor C_1 is 2200μF, and the resistance of load R_1 is 10Ω. The

frequency of PWM signal is 5kHz. All those parameters in the simulation model were initially given based on the author's experience; after several simulations, they were eventually confirmed.

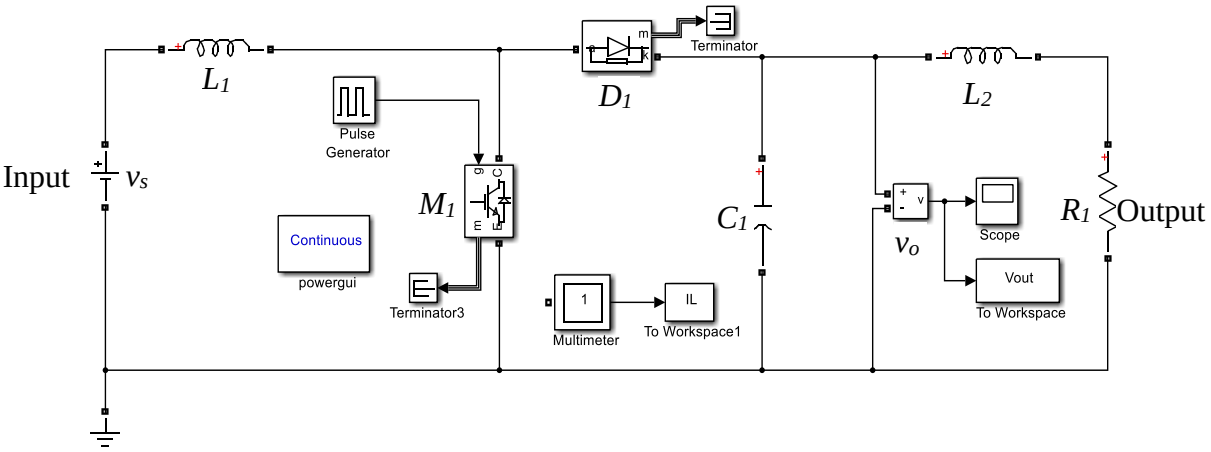


Figure 5- 4 Conventional boost circuit model

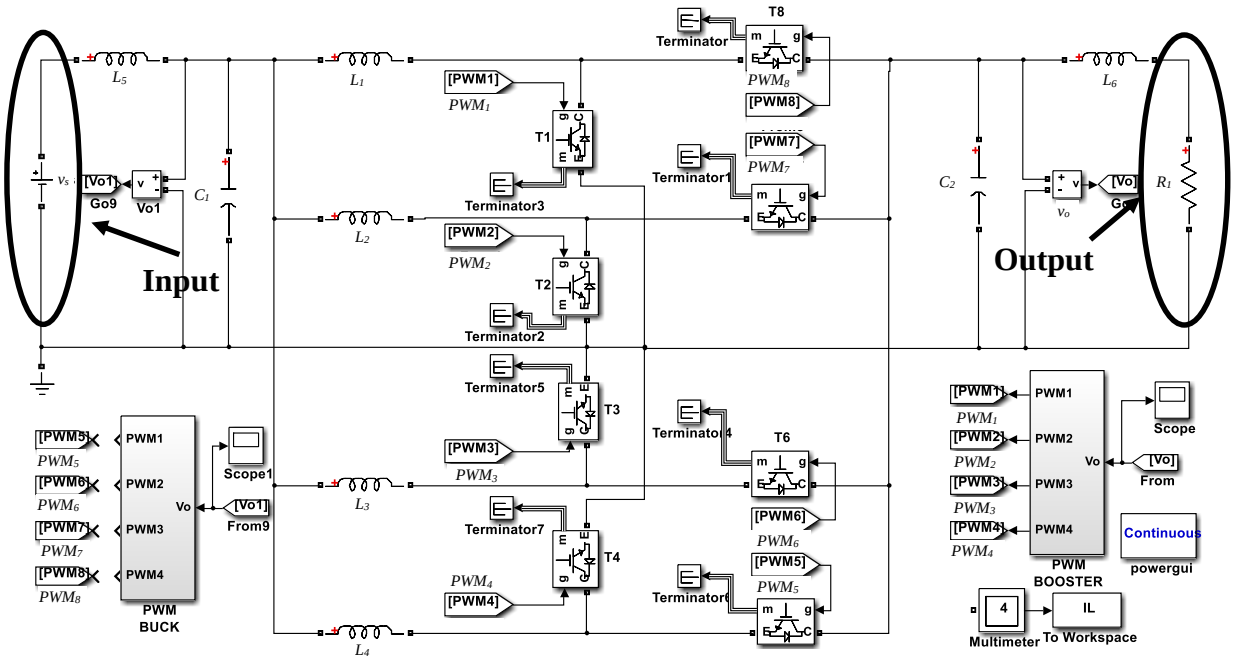


Figure 5- 5 Simulation of four-phase IBDBBC circuit

Figure 5-5 shows a four-phase IBDBBC operating under boost mode. In the simulation model, all the parameters of the components in the circuit are the same as in Figure 5-4. The frequency of the controlled PWM signals is 5kHz, v_s is considered as an input battery bank with a nominal

voltage 200Vdc, the R_1 10Ω is the load of the circuit, which can be considered as a higher potential DC bus, so the expected output voltage of the boost converter is 450V. The inductances of the input and output filter inductors L_6 and L_5 are 50μH each, filter capacitors C_2 and C_1 are 2200μF each, and the inductance of energy stored inductors L_1-L_4 are 200μH each. The blocks of PWM Boost and PWM Buck generate four-phase PWM signals for boost mode and buck mode respectively.

In Figure 5-5, the circuit operates under boost mode which means power can be delivered from the low potential side to the high potential side when PWM_1-PWM_4 are activated and PWM_5-PWM_8 are disabled. Conversely, swapping the input and output side, enable PWM_5-PWM_8 and disable PWM_1-PWM_4, the circuit operates under buck mode.

Figure 5-6 illustrates the four-phase PWM signals generated by the block of PWM Boost for boost mode operation, in which, the PWM signals are out of phase 90^o to each other.

The simulation result of the current flowing through the energy stored inductor in the conventional boost topology is shown in Figure 5-7. As the simulation result in Figure 5-7 shows, the maximum peak current carried by the inductor reached roughly 75A. Comparing this with the results of four-phase IBDBBC circuit shown in Figure 5-8, the current flowing through each inductor is significantly reduced and the average current of each inductor is approximately reduced by about 50%. This means the thermal dissipation (I^2R losses) problems of the electronic components are considerably reduced.

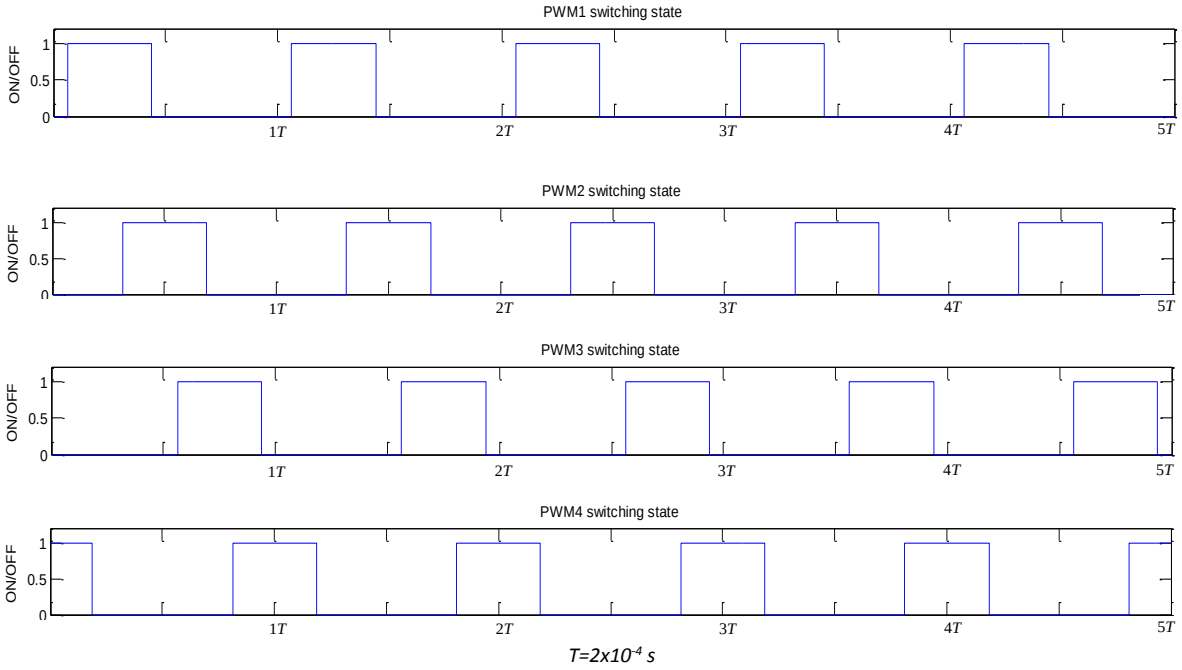


Figure 5- 6 Generated PWM signals

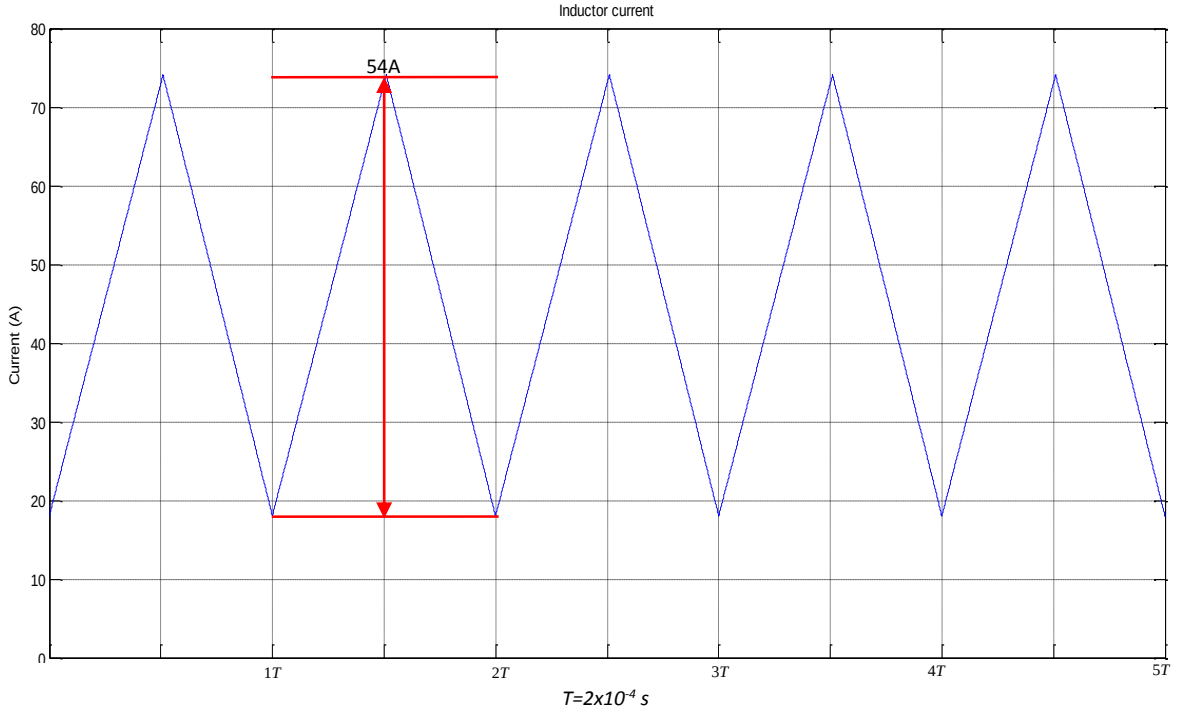


Figure 5- 7 Inductor current of conventional CCM boost circuit

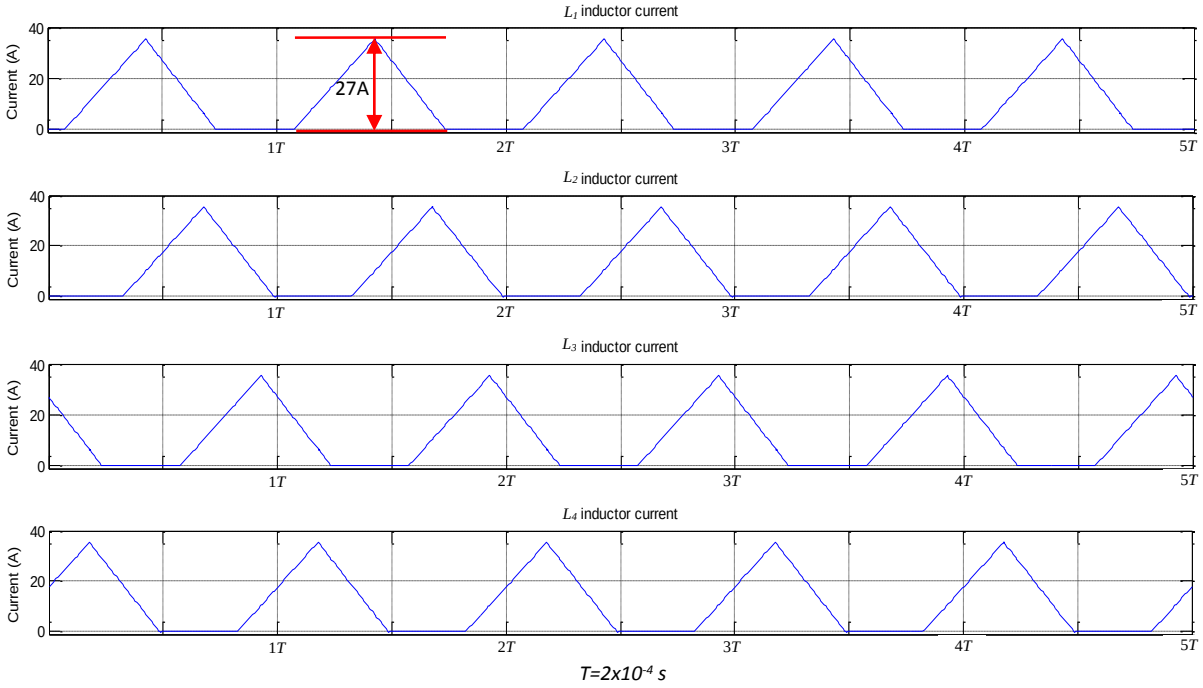


Figure 5- 8 Inductor currents of IBDBBC circuit

Figure 5-9 and 5-10 show the simulation results of the output DC voltage of the conventional boost and the four-phase IBDBBC circuit, respectively.

As Figure 5-9 illustrates the voltage output of the conventional boost circuit has a ripple voltage of about 2.25V. By contrast, the output from the IBDBBC circuit only has a ripple voltage of about 0.2V, as shown in Figure 5-10. This means the output power quality of four-phase IBDBBC is much better than conventional boost.

Additionally, in the simulation results of the four-phase IBDBBC circuit, the frequency of ripple voltage is 4 times that of a conventional boost circuit. That means the output ripple voltage can be filtered easily with a relatively small size capacitor.

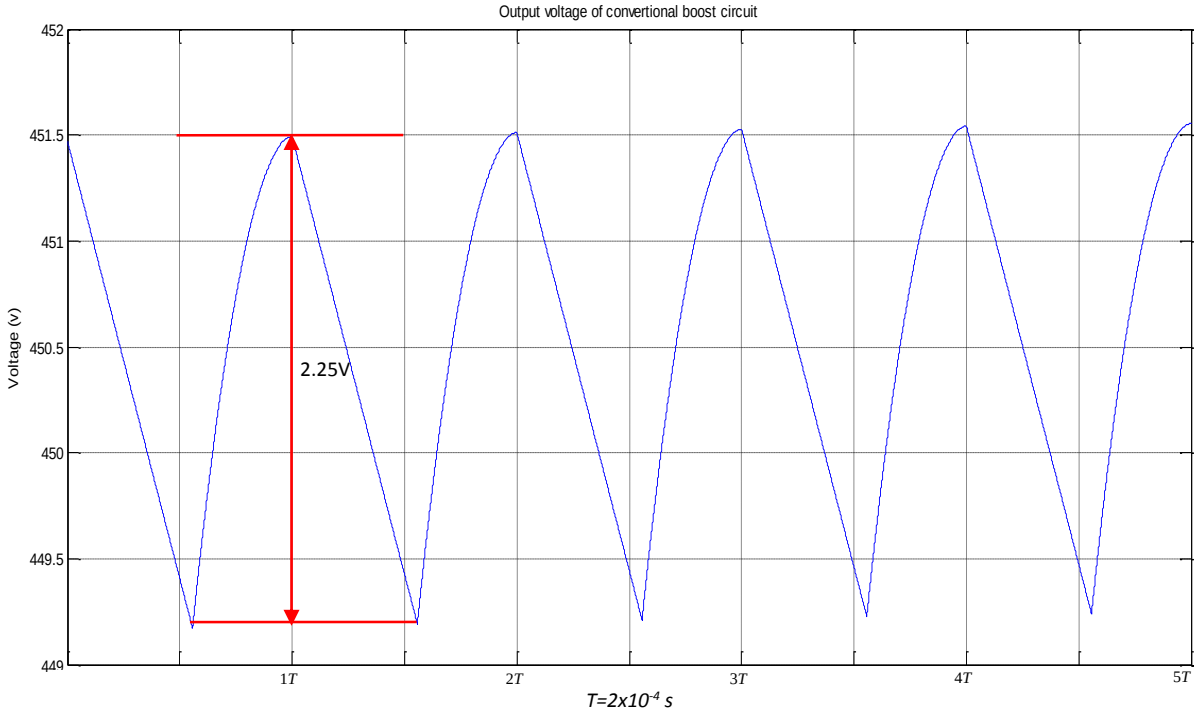


Figure 5- 9 DC output voltage of conventional boost circuit

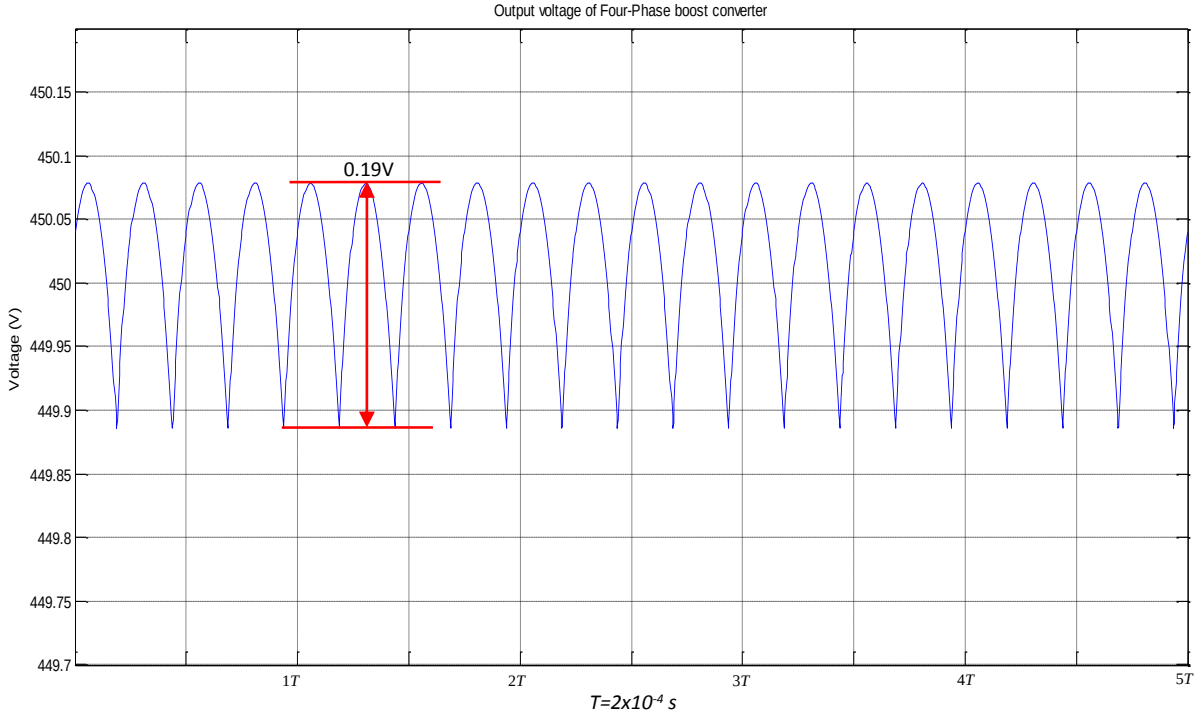


Figure 5- 10 DC output voltage of four-phase IBDBBC circuit

5.6 Modelling four-phase IBDBBC under buck mode

Figure 5-11 illustrates a simulation model of the IBDBBC operating under buck mode, the switching signals PWM5-PWM8 are enabled and PWM1-PWM4 are disabled, which means the input terminals and output terminals are conversely changed comparing with Figure 5-5. All the parameters of the components and the simulation conditions are exactly the same as under boost mode which was described in the previous section and shown in Figure 5-5. In order to observe the response of converter output voltage, at the point of 0.2s, input voltage steps up from 350Vdc to 450Vdc. In order to compare with interleaved boost circuit in Figure 5-5, most devices in the figure remains unchanged but the PWM control signals, and the input and output terminals are swapped.

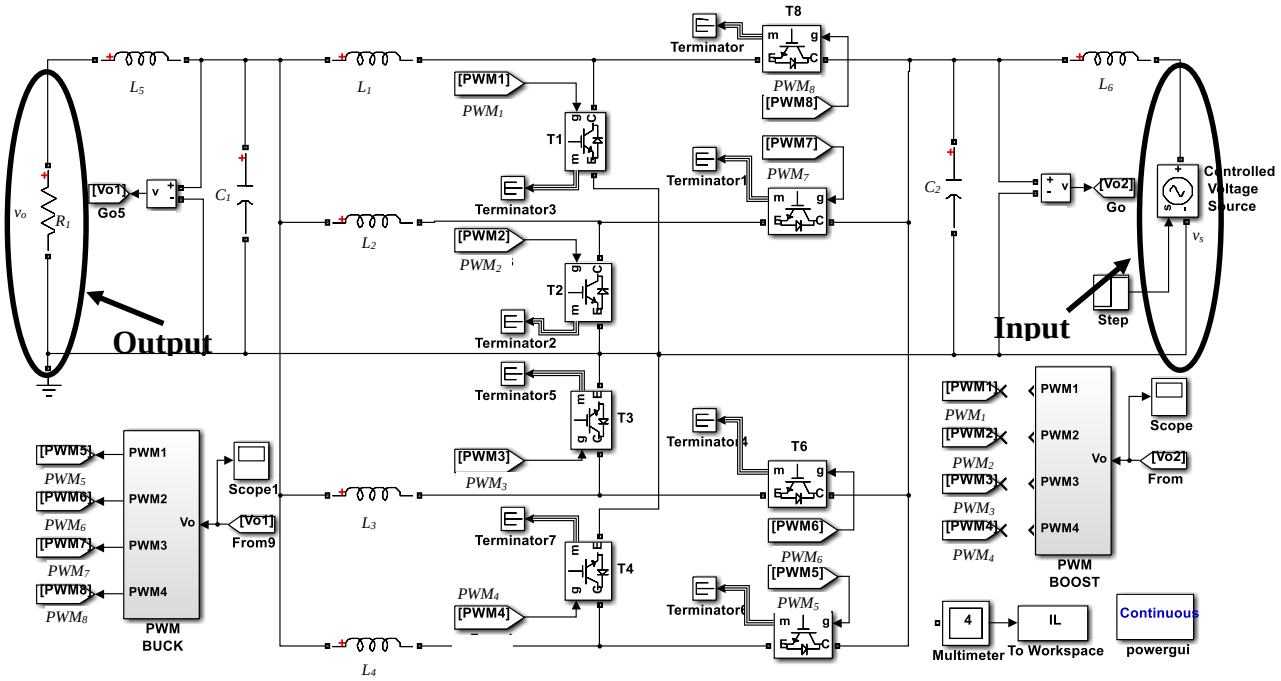


Figure 5- 11 Simulation of four-phase IBDBBC under buck mode

The simulation results for the input and output currents of the interleaved buck converter are shown in Figure 5-12. It can be seen that the output current is continuous and input current is discontinuous.

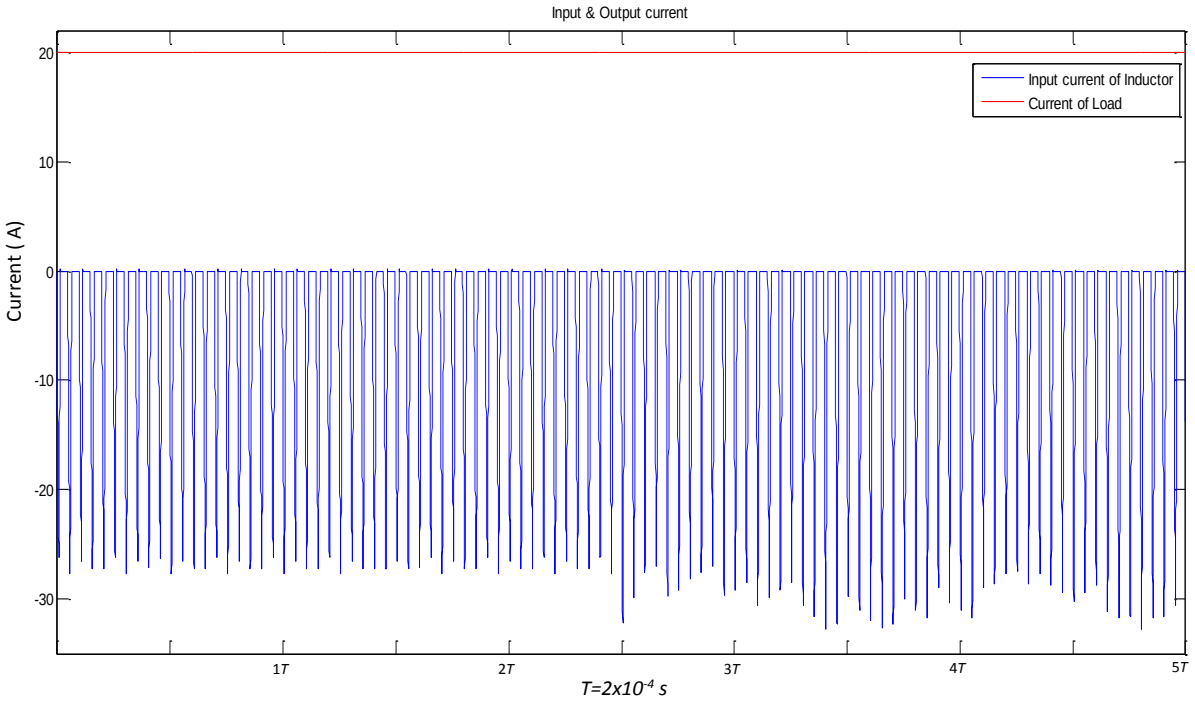


Figure 5- 12 Input and output current

The voltage of a battery bank is generally more stable than the DC bus voltage due to the intermittent character of the renewable energy source which causes the generator output with fluctuation. Figure 5-13 illustrates that the charging voltage at the battery terminal remains almost constant at approximately 200Vdc when the DC bus voltage steps up from 350Vdc to 450Vdc.

Figure 5-14 demonstrates that the output ripple voltage of the four-phase IBDBBC operating under buck mode remains relatively small when the input steps up from 350V to 450V. The ripple increases from approximately 0.06V to around 0.15V.

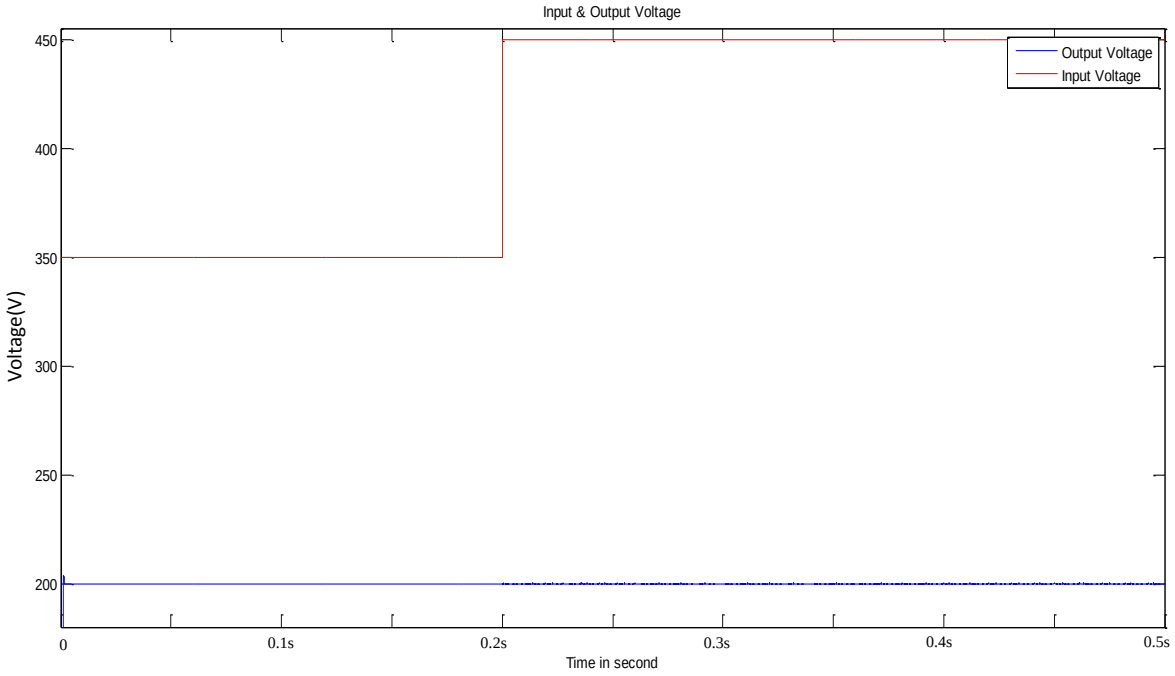


Figure 5- 13 Input and output voltage

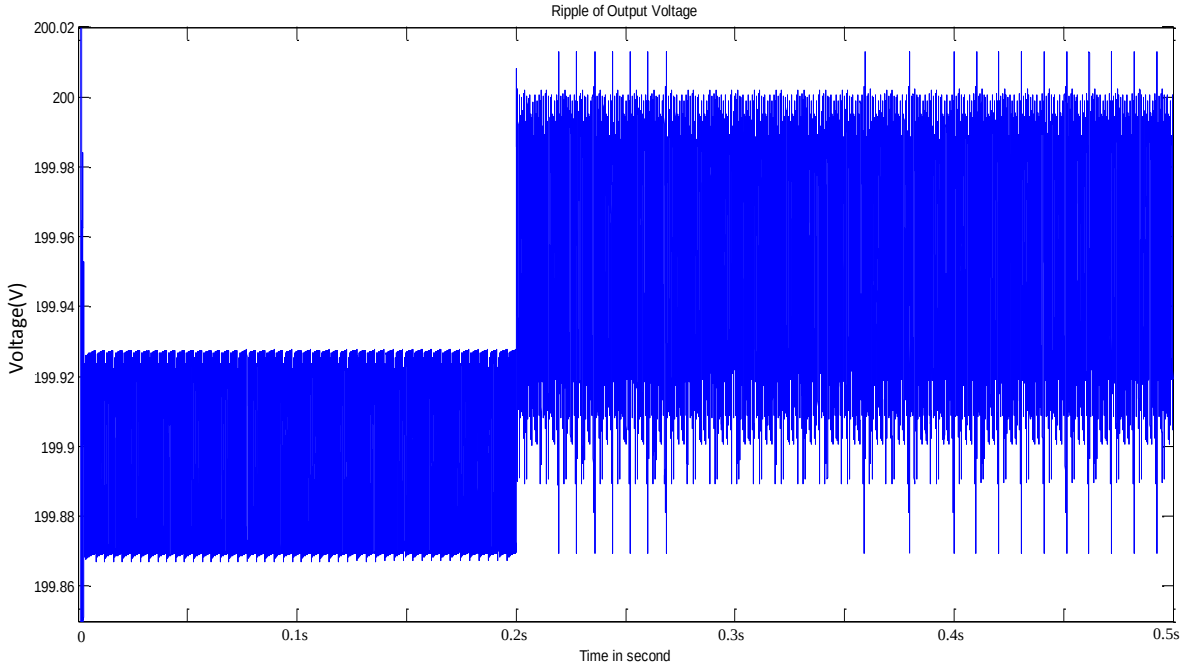


Figure 5- 14 Output voltage ripple

5.7 Summary

A novel four-phase IBDBBC to deal with the bi-directional power flow between a DC bus and a battery bank has been proposed, designed, modelled and simulated. Comparing this design with the conventional boost-buck converter, the four-phase IBDBBC can significantly reduce the ripple of output voltage, the thermal dissipation and the current stress on the switching devices.

Chapter 6 GCI with RPC

6.1 Introduction

This chapter presents a novel control strategy for a single-phase inverter to achieve RPC and output active power when the inverter is connected to a single-phase electricity grid. Because the SOGI introduced in Chapter 3 can produce a pair of orthogonal signals, it is used to construct an orthogonal current signal for splitting active and reactive current based on the instantaneous load current sampled from the single-phase grid. The active and reactive current of the grid can be rapidly decomposed through trigonometric calculation. The reference current of the inverter output can be produced through the actual active and reactive currents which are obtained in the previous stage. Then the re-synthesised reference current is compared with the inverter output current, and the difference is used to generate the PWM signals for controlling the IGBT devices.

The GCI is one of the most important parts of a distributed generator using renewable energy sources. The power output from solar PV panels is DC, so the inverter plays a key role to convert DC to AC power. Although most wind turbines generate AC power, however, the AC power generated by wind turbines cannot be fed directly into the power grid. For example, wind turbines with synchronous generators output AC power with variable frequency due to constantly changing wind speed, and the variable frequency AC power must be converted to a fixed frequency AC power through AC/DC and DC/AC conversions for grid connection.

The conventional GCI interfacing a renewable power generator and the electricity grid is generally equipped with an MPPT algorithm which is expected to draw maximum power from the renewable source. However, the conventional GCI has some critical issues. Firstly, the inverter injects maximum power into the grid with the fluctuation of renewable energy sources

without providing RPC. Secondly, the inverter feeds the power to the grid as much as it can without considering the grid condition (such as voltage, frequency and power factor) and power demand on the grid.

Based on their applications, the inverters for renewable power generators can be categorised into standalone inverters and GCIs. Generally the characteristic of a standalone system is equipped with an energy storage which can be used to maximally extract energy from the renewable sources and consistently provide power for loads while smoothing or even eliminating renewable source fluctuation. Most GCIs without energy storage devices consider the utility grid as a battery of unlimited capacity. The conventional GCI is generally composed of an MPPT block, PLL block and DC/AC inverter block. The MPPT is realised to ensure maximum power from the renewable source at any time, PLL block is used to synchronise the inverter power output with power grid voltage, and DC/AC inverter is tasked to feed the power generated by the renewable power generator into the grid.

Initially, the technology of standalone inverters and GCIs gradually evolved from the application of VFD, where AC power supply with variable frequency is required to improve performance, such as for an induction motor. Hence, the control algorithms of an RES inverter is similar to that for a VFD.

The GCI can be considered as an interface device between the RES and the grid. There are a number of of topologies and control methodologies which have been implemented in the last two decades. With the historic development of GCIs in the area of solar PV power systems, they can be divided into three types: centralised inverter, string inverter and multi-string inverter (Kjaer, et al., 2005). Additionally, based on whether the inverter has a transformer or not, the GCI can also be categorised as a transformer inverter or transformerless inverter.

The centralised inverter operates between the grid and large number of solar PV panels connected in series strings to produce adequate voltage. The series strings are connected in parallel through anti-reverse current diodes. The major drawback of this type of system is that the plant with central inverter shuts down if any problem occurs in the inverter. A further drawback is that the effect of shading using centralised inverter is worse than when using string inverters. For example, when clouds gather over a solar power farm, the performance and effectiveness of the system using string inverters is better than for a centralised inverter system. Although the string-inverter technology can reduce the power losses on the DC bus, however, it treats group's panel as a single large panel, any problems of single panel could impact whole system performance. The technology of multi-string systems is an advanced development of string-inverter systems, in which each string has its own DC to DC converter with MPPT supplying power to the DC bus link and from there then injects AC power into the utility grid via a common inverter. All the inverter systems discussed above inject the maximum possible power into the electricity grid, even in the situation of that the capability of utility grid provided matched customer's electricity requirement. Also, it is rare that a GCI can quantitatively provide RPC.

6.2 Topologies of a GCI

For a DC/AC inverter, according to its AC output waveforms, it can be considered as a VSI, where the independently controlled AC output is the voltage waveform. Alternatively, it can be considered as a CSI, where the independently controlled AC output is the current waveform (Espinoza, 2001). There are a number of methods and techniques which are widely utilised to implement VSIs and CSIs. According to the PWM carrier wave, the methods are classified into many types, such as Square-wave Operation, Carrier-based PWM, Switch Frequency Optimal (SFO)-PWM, Regular and Non-regular Sampled PWM, Selective Harmonic Elimination PWM (SHEM), SVPWM (Amatoul, et al., 2012) (Espinoza, 2001) and Hysteresis Current Control

(HCC) (Bode & Holmes, 2000). HCC has the advantage of an inverter output with small output current ripples, and it is a real time control methodology with very good stability, close tracking of current requirements and rapid transient response (Kojabadi, et al., 2006). Hence, HCC is widely used for single-phase GCIs.

According to practical applications, GCIs can be categorised as single-phase VSI, three-phase VSI, single-phase CSI and three-phase CSI. The inverter can be divided into half-bridge and full-bridge on the basis of the number of inverter legs. The topologies of a half-bridge VSI and a full-bridge VSI, based in a single-phase system are shown in Figures 6-1 and 6-2 respectively. In Figure 6-1 the two large capacitors provide a central neutral point for the load. That implies the voltage across each capacitor should be equal to half voltage supply $v_s/2$.

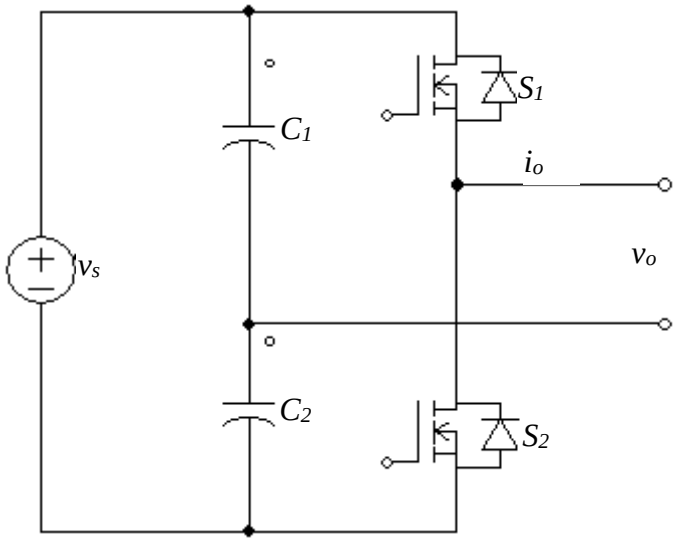


Figure 6- 1 Topology of half-bridge single-phase VSI

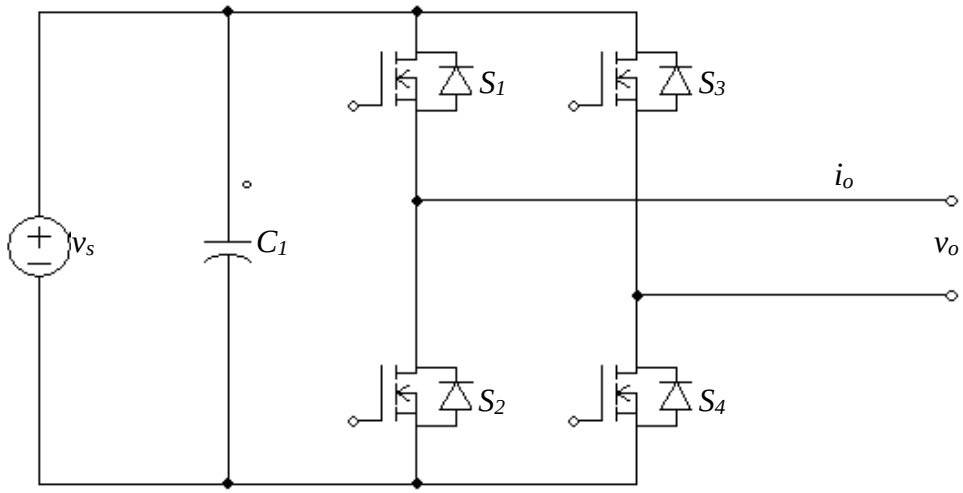


Figure 6- 2 The topology of full-bridge single-phase VSI

In the full-bridge single-phase VSI, illustrated in Figure 6-2, an additional leg of switches (controlled in anti-phase) is utilised to replace the neutral point. In both the half-bridge VSI and the full-bridge VSI, the top switch and bottom switch in the same leg are not allowed to be switched "on" simultaneously. If switching devices S_1 and S_2 (or S_3 and S_4) are switched "on" at the same time, this would create a short circuit across the DC power supply, v_s.

6.3 GCI based on HCC

Figure 6-3 shows the block diagram of generally grid-connected single-phase inverter based on close-loop HCC. The PLL block produces normalised sinusoidal signal which is synchronous with power grid. The inverter output targeted current I_{Ref} multiply PLL output to generate instantaneous reference current, i_{Ref}. The generated instantaneous reference current i_{Ref}, is compared with the output current of the inverter i_o to yield an offset error signal, Δi, which is the input of the hysteresis controller. According to the extent of the offset error, the controller determines which pair of the switching devices S_1 and S_4 or S_2 and S_3 should be switched "on" or "off". If i_{Ref} is positive, the output current of the inverter will be increased as the switching devices S_1 and S_4 are switched "on" (with S_2 and S_3 switched "off"). Conversely, the current will be decreased as S_2 and S_3 are switched "on" (with S_1 and S_4 switched "off"). If

i_{Ref} is negative, switching "on" S_1 and S_4 (with S_2 and S_3 switched "off") will cause the absolute value of i_o to be decreased, otherwise it will be increased. To summarise the above analysis, the output current of the inverter will be increased when S_1 and S_4 are switched "on" (with S_2 and S_3 switched "off"); switching "on" S_2 and S_3 (with S_1 and S_4 switched "off") will cause the output current of the inverter to be decreased. Therefore, if the hysteresis band is set as $2\Delta i$, then the output current is between $i_{Ref}+\Delta i$ and $i_{Ref}-\Delta i$.

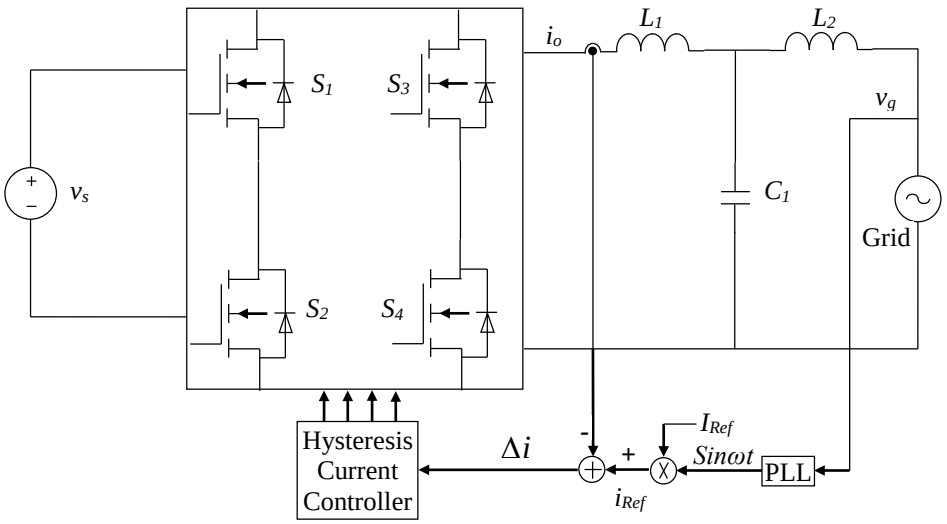


Figure 6- 3 Structure of DC/AC inverter based on HCC

6.4 Simulation of conventional single-phase GCI

The output voltage of the inverter has to be synchronised with the grid voltage, which means it is essential to embed the function of PLL in the inverter for tracking the phase angle of the grid voltage.

Assume the grid voltage is

$$v = A\sin\omega t \qquad (6-1)$$

where A is the amplitude of the grid voltage, ω is the angular frequency of the grid voltage.

Taking derivative with respect to time from Equation (6-1) yields:

$$\frac{dv}{dt} = A\omega \cos \omega t \qquad (6-2)$$

The tangent of instantaneous phase angle of the grid voltage can be obtained as:

$$\tan \theta = \frac{v\omega}{dv/dt} = \frac{A\omega \sin \omega t}{A\omega \cos \omega t} = \tan \omega t \qquad (6-3)$$

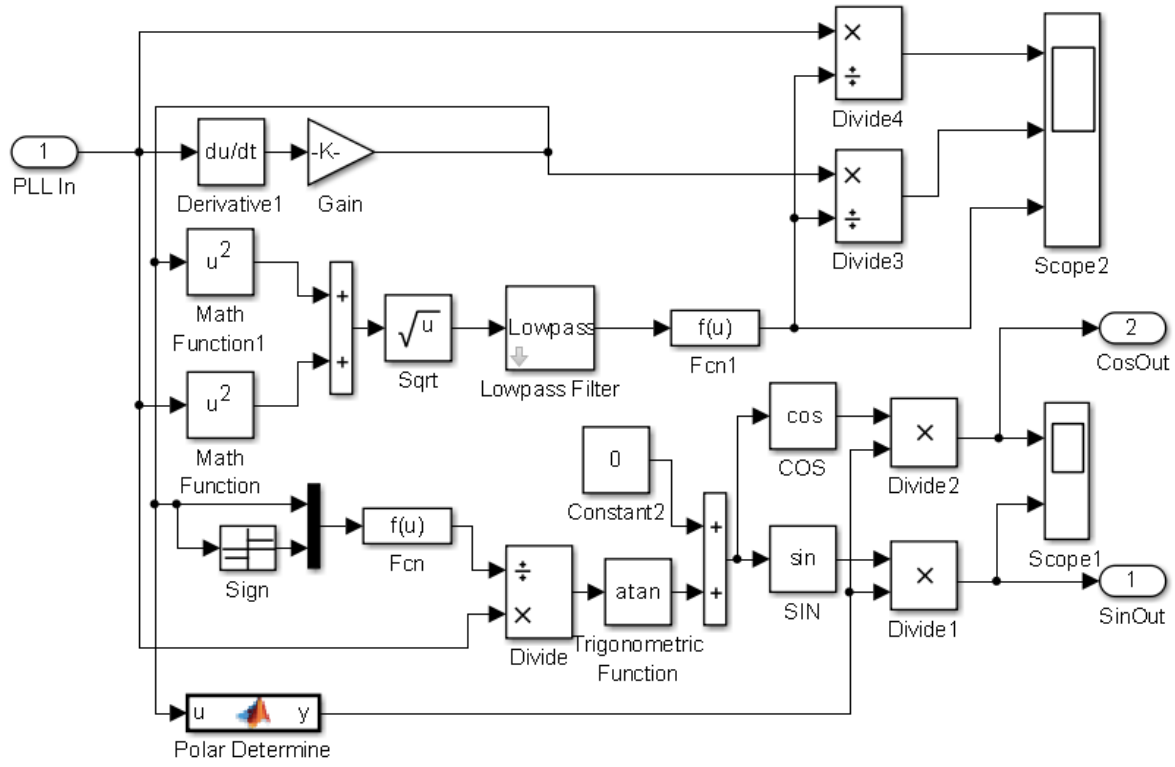


Figure 6- 4 Simulation model of conventional PLL for GCI

Figure 6-4 is the simulation block diagram which is utilised to implement the PLL function for GCI according to Equations (6-1) to (6-3).

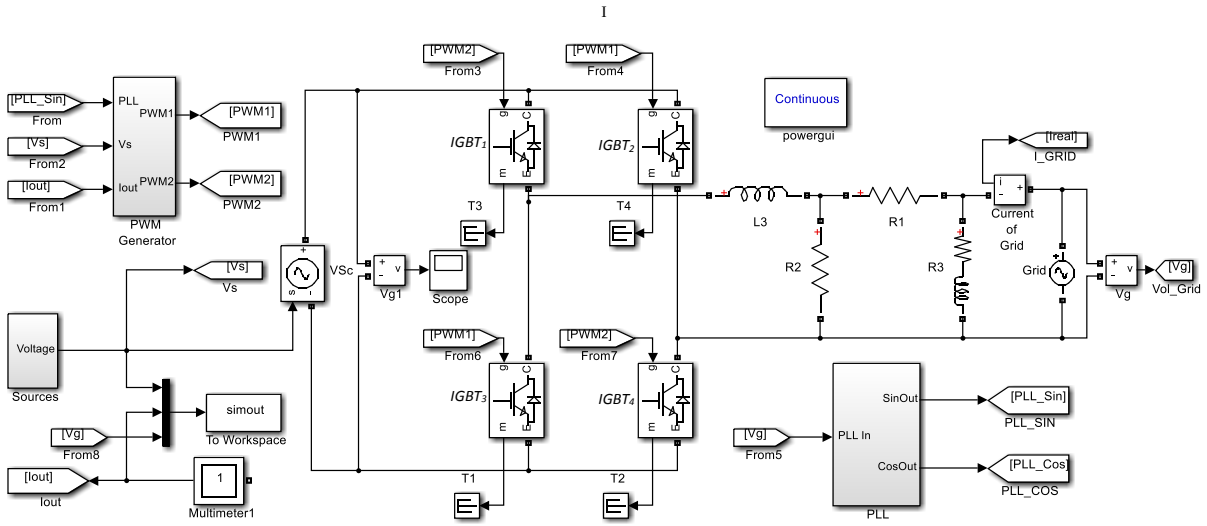


Figure 6- 5 Simulation model of full-bridge single-phase GCI

Figure 6-5 is the complete simulation model of a full-bridge single-phase GCI with hysteresis control (bang-bang). In the figure, the inverter-bridge is formed by 4 IGBTs, $IGBT_1$, $IGBT_2$, $IGBT_3$ and $IGBT_4$. The block of PLL takes instantaneous voltage of the grid as input signal to attain normalised sine and cosine values of the grid voltage phase angle. The block of PWM Generator produces 4 channels of control PWM signals for the inverter-bridge in accordance with input voltage, the phase angle of grid voltage and the output current of the inverter. The block of Source generates a dynamically varying DC power supply to simply simulate PV panel output with fluctuation.

In order to observe changes of the inverter output as the voltage on the DC bus varies, an input voltage source is provided, as shown in Figure 6-6 (a). Figure 6-6 (b) shows the output current of the inverter. The amplitude of output current of the inverter varies as a result of the changes of the input voltage.

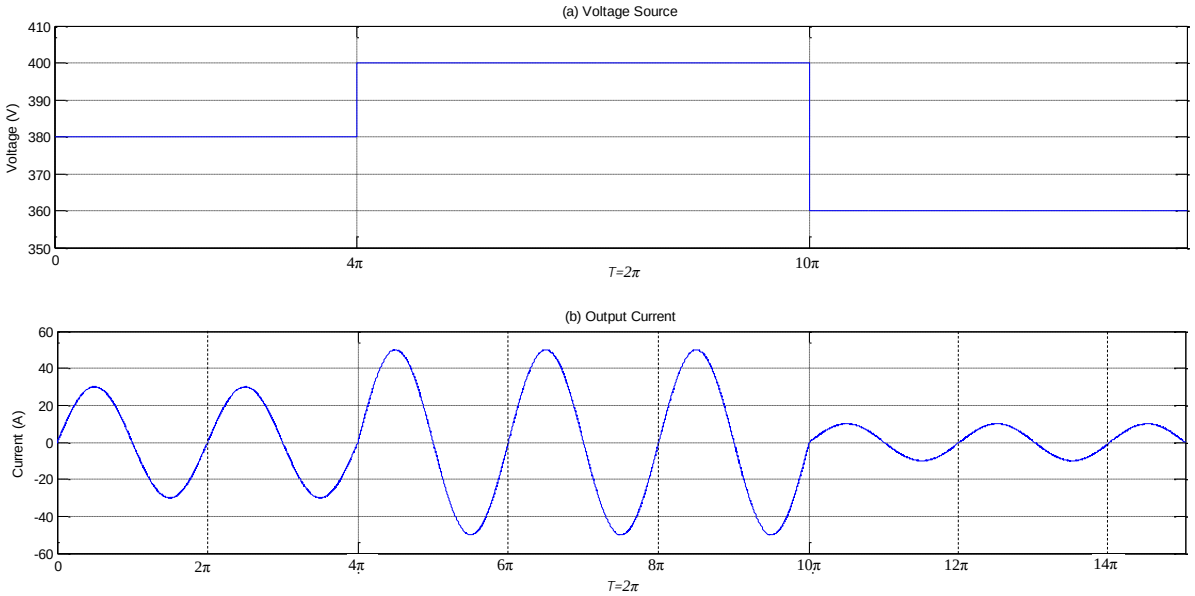


Figure 6- 6 Simulation results of full-bridge single-phase GCI

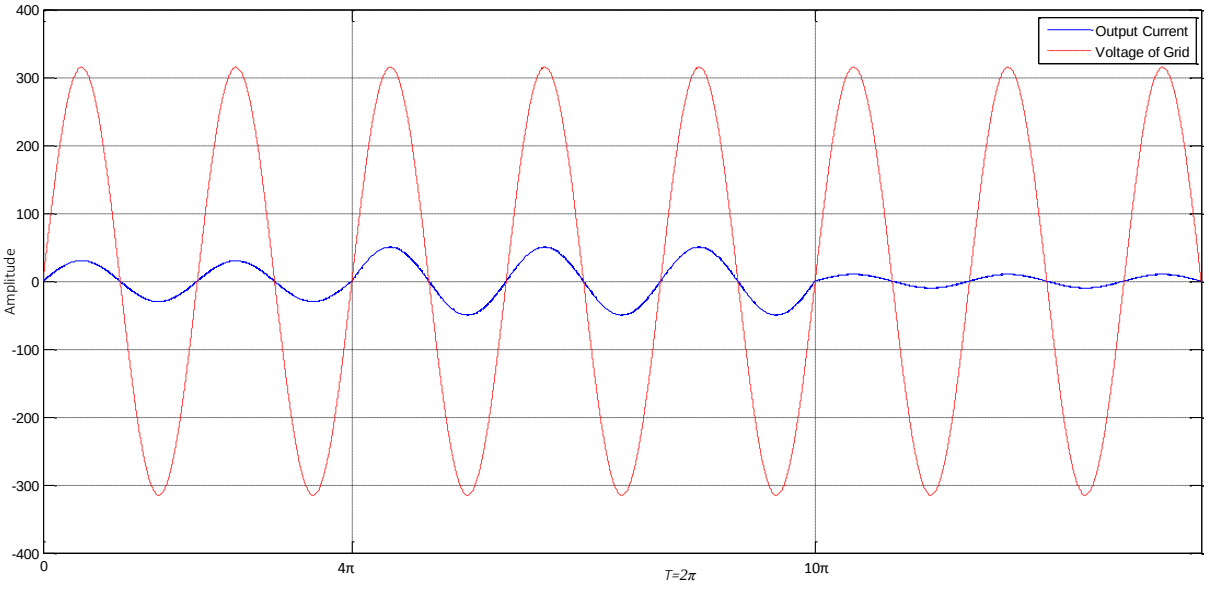


Figure 6- 7 Output current of conventional GCI

Figure 6-7 illustrates the relationship between the grid voltage and the output current of the inverter. The output current is in phase with the grid voltage, i.e. there is no reactive power injection to the grid from the inverter.

Through analysing the simulation results as shown in Figure 6-6 and 6-7, it can be said that inverter output current follows the changes of the voltage on the DC-bus, and output current is in phase with the grid voltage.

6.5 RPC

This section presents a novel algorithm to deliver quantitative RPC for a micro-grid.

The conventional STATCOM is generally connected to the grid in parallel with a load. The output reactive power and current of the STATCOM can be controlled by means of adjusting either the voltage at the PCC, or the amplitude and phase angle of the current outputted from STATCOM.

Supposing a smart micro-grid system is installed in a community, which comprises a number of small scale distributed generators (SSDG) with RPC, a central controller, current and voltage transducers, and a communication system. A stable and secure generation system should guarantee that residents in the community are not affected by unpredictable power cut off from the main grid. Therefore, the whole system without grid support should deliver both active power and reactive power to meet the power demands of the community. A single small scale SSDG, in a smart micro-grid, is not capable of completely compensating the whole micro-grid system's reactive power. However, the whole system's reactive power may be compensated collectively by all the SSDGs, because each SSDG can deliver a certain amount of reactive power.

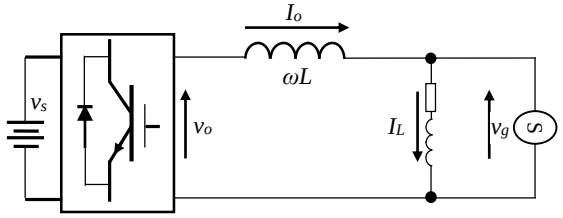


Figure 6- 8 Schematic diagram of GCI

Figure 6-8 shows an equivalent schematic of a single-phase GCI which is connected into the power grid through an output filter inductor with inductance ωL.

Generally, the impedance of an electricity grid is inductance, which means the grid as a load consumes reactive power, and the load's current lags the voltage with a certain phase angle. Therefore, if the inverter output current leads the grid voltage with a certain same phase angle, then the grid reactive power can be compensated.

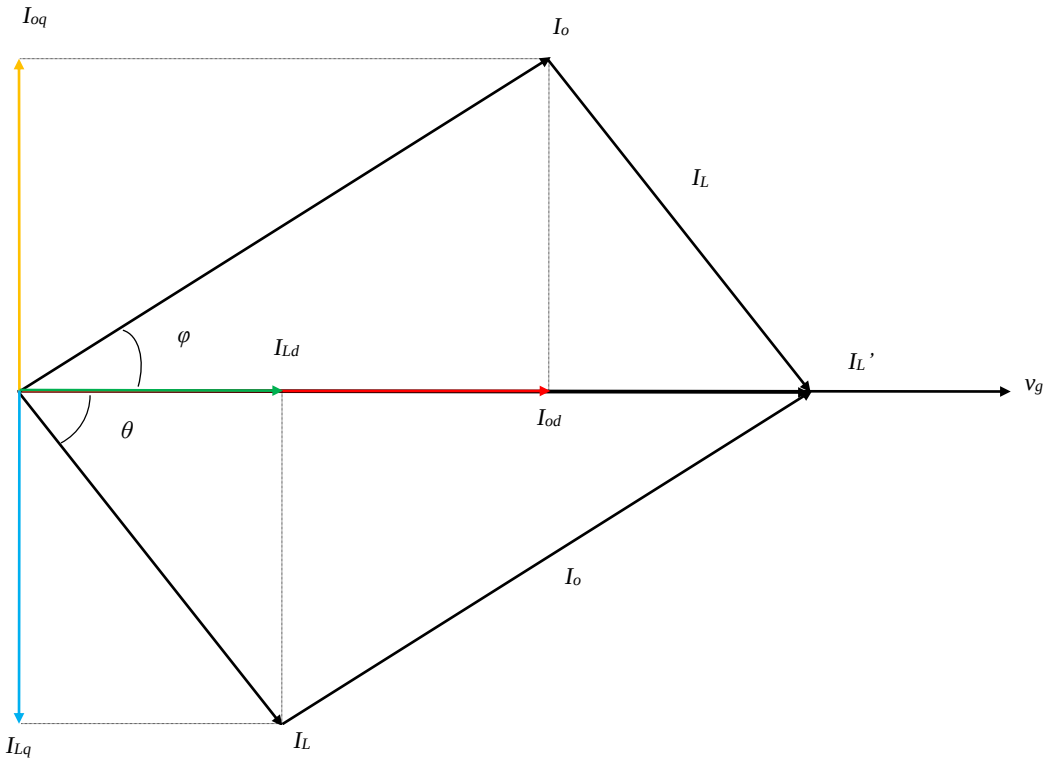


Figure 6- 9 Vector relationships of GCI

Figure 6-9 illustrates the vector relationships between the output current I_o of the inverter, the load current I_L and the grid voltage v_g. In Figure 6-9, the load current I_L is lagging by a phase angle θ with respect to the grid voltage v_g. The load current can be decomposed into active and reactive currents I_{Ld} and I_{Lq} respectively. Figure 6-9 illustrates that if the inverter output current I_o is composed by an active current component I_{od} and a reactive current component I_{oq}, which is equal in magnitude to the load reactive current component I_{Lq} but opposite in phase to I_{Lq},

the whole system's reactive power can be completely compensated by the inverter, thereby achieving the objective to inject active power to the grid with RPC.

6.5.1 Control strategies

The theory of instantaneous active and reactive power is the well-known p-q theory which is most widely used in time-domain reference current generation techniques (Golestan, et al., 2013; Wang, et al., 2007). The SOGI is widely exploited to achieve PLL (Golestan, et al., 2013) (Rodriguez, et al., 2009) (Fedele, 2012) and to eliminate, or reduce, the instantaneous noise level in many fields, such as control theory, relaying protection, signal processing, radio frequency, power systems. (Fedele, 2012). In the present study, SOGI is utilised to construct a pair of orthogonal trigonometric functions for the load current in a single phase system, which is sampled at the PCC of the micro-grid, as shown in Figure 6-10.

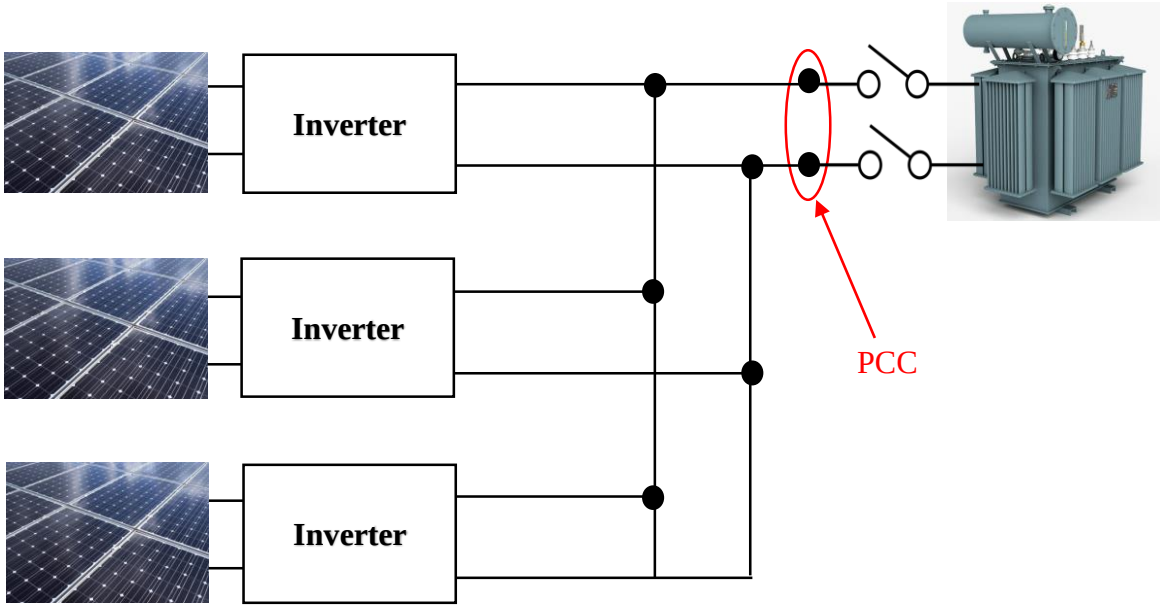


Figure 6- 10 PCC of single-phases system

As previously discussed in chapter 4, instantaneous active and reactive power can be represented as Equation (4-4). In the equation, as $i_{q,}$ the q-axis component of the grid current, approaches 0, the reactive power component Q approaches 0 and only the d-axis component,

$v_d i_d$, the active power term remains. Through analysis of the above equation, the reactive power Q of the power grid can be controlled by adjusting i_q, the instantaneous quadrature component of current, in the d-q rotating frame.

Through the above analysis, the reactive and active power can be regulated by adjusting components of i_d and i_q individually. The *d*- and *q*- axis components can be obtained by means of transformation from the stationary frame, and those two signals are an orthogonal pair of the load currents. Therefore, for a single-phase system, it is necessary to construct a pair of orthogonal signals from the load current as Figure 6-11 illustrates.

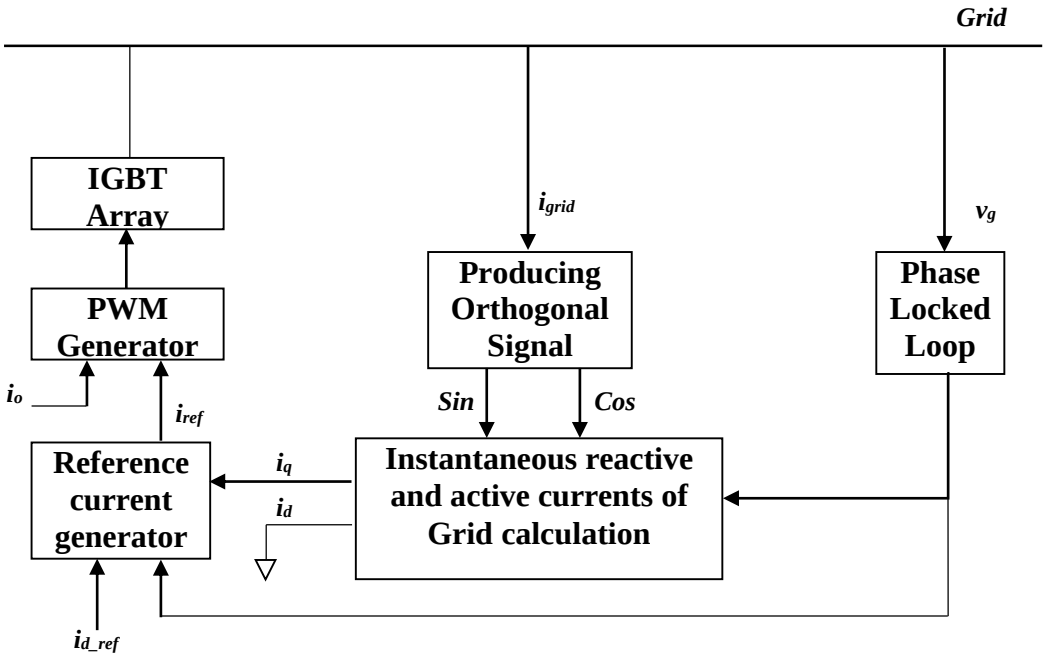


Figure 6- 11 Structure of control algorithm

The single-phase instantaneous voltage of the power grid and the load current are given by:

$$v_g = v_{max} \cos \omega t \tag{6-4}$$

$$I_\alpha = I_{max} \cos(\omega t - \theta) \tag{6-5}$$

where

v_{max} is the peak value of the grid voltage.

I_{max} is the peak value of the load current.

I_{α} is the instantaneous load current.

θ is the phase angle of the load current respect to the grid voltage.

The orthogonal component of the instantaneous load current in Equation (6-5) can be obtained as:

$$I_{\beta} = I_{max}\, sin(\omega t - \theta) \tag{6-6}$$

Conducting trigonometric calculation for Equations (6-5) and (6-6) yields:

$$I_{\alpha} = I_{max}\, cos\, \omega t\, cos\, \theta + I_{max}\, sin\, \omega t\, sin\, \theta \tag{6-7}$$

$$I_{\beta} = I_{max}\, cos\, \omega t\, sin\, \theta - I_{max}\, sin\, \omega t\, cos\, \theta \tag{6-8}$$

$$\begin{bmatrix} I_{\alpha} \\ I_{\beta} \end{bmatrix} = \begin{bmatrix} cos\, \omega t & sin\, \omega t \\ -sin\, \omega t & cos\, \omega t \end{bmatrix} \begin{bmatrix} I_{max}\, cos\, \theta \\ I_{max}\, sin\, \theta \end{bmatrix} \tag{6-9}$$

To obtain the active and reactive load current by multiplying both sides of Equation (6-9) by the matrix $\begin{bmatrix} cos\, \omega t & -sin\, \omega t \\ sin\, \omega t & cos\, \omega t \end{bmatrix}$ gives

$$\begin{bmatrix} I_{max}\, cos\, \theta \\ I_{max}\, sin\, \theta \end{bmatrix} = \begin{bmatrix} cos\, \omega t & -sin\, \omega t \\ sin\, \omega t & cos\, \omega t \end{bmatrix} \begin{bmatrix} I_{\alpha} \\ I_{\beta} \end{bmatrix} \tag{6-10}$$

From Equation (6-10), the active current i_d and reactive current i_q are decomposed from the load current given in Equation (6-5), which are $I_{max}cos\theta$, $I_{max}sin\theta$ respectively.

Figure 6-12 illustrates a block diagram of RPC for a single-phase system, which is based on the above equations. The control system takes instantaneous samples of grid voltage v_g and the load current of grid i_g, calculates the reactive power current component i_q which is used to

combine with the demanding active power current i_{d_re} to generate a reference current i_{ref} for the inverter output.

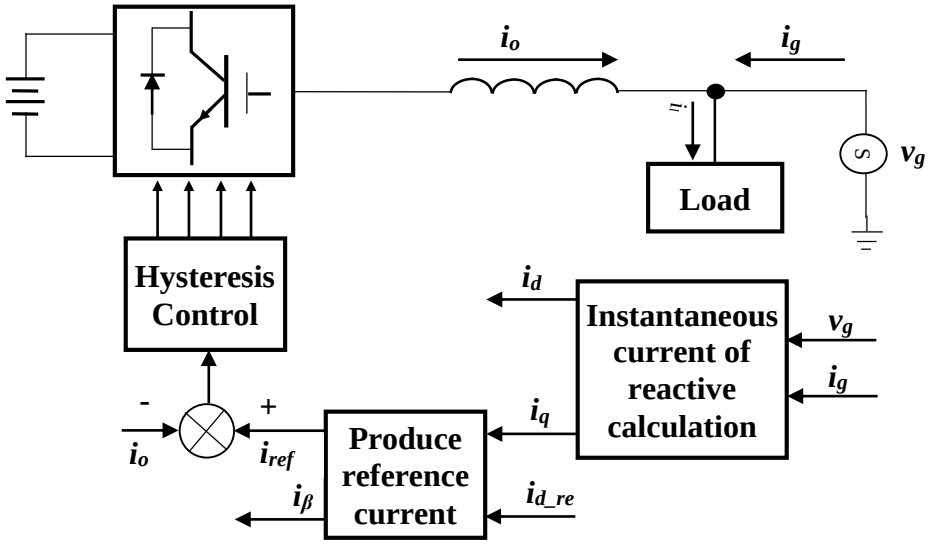


Figure 6- 12 Diagram of RPC

The sine and cosine functions in Equation (6-10), can be provided by a PLL module, as illustrated in Figure 6-13, which is a module designed to obtain instantaneous active and reactive power from the grid. The block of the Orthogonal Generator in Figure 6-13 is an SOGI module introduced in Chapter 3, which is employed to generate a pair of orthogonal signals according with sampling current signal i_g.

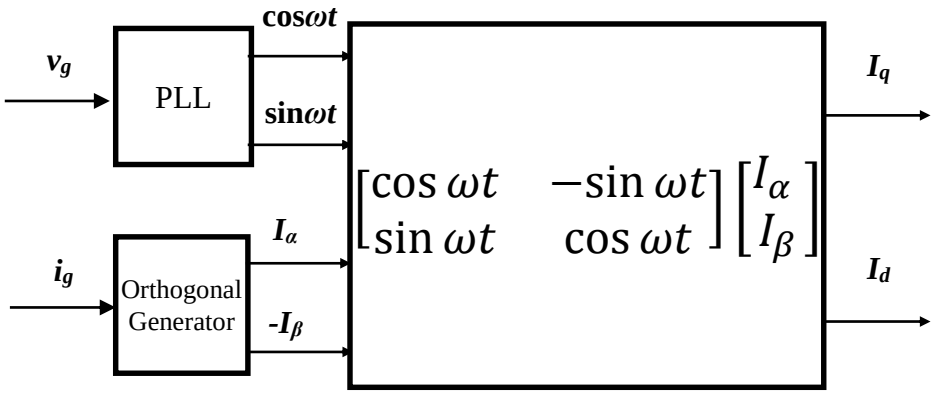


Figure 6- 13 Split instantaneous active and reactive current

The system samples the grid voltage to ensure the voltage output of the inverter is completely synchronous with the grid in the terms of frequency, phase angle and the root mean square (RMS) value.

Figure 6-14 implements Equation (6-9), which illustrates that the module produces the output reference current of the inverter according to the demanding reactive current i_g obtained from the grid current, the inverter providing active current i_{d_def} in accordance with instructions from the control centre , and the PLL signals.

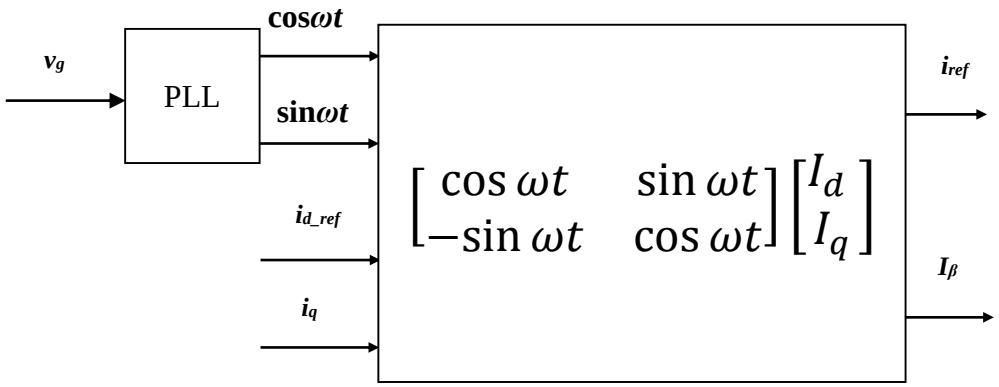


Figure 6- 14 Generated reference current

6.6 Simulation of single-phase GCI with RPC

Figure 6-15 illustrates a MATLAB/Simulink model of a single-phase GCI with RPC, which is based on the diagram shown in Figure 6-12. In the simulation model, the PLL block assures the GCI output voltage is synchronous with the grid voltage. The block labelled D_Q decomposes the grid current to obtain the reactive and active components of the grid current. The I_REF block combines the reactive current component and demands the active current component to generate a reference current for the GCI output. The inverter output current is fed back to and compared with the generated reference current to produce the PWM control signals for the inverter-bridge.

In the simulation model, R_1 represents the equivalent sampling impedance of output current and the resistance of R_1 is 1Ω; L_3 is the filter inductor at the inverter output and the inductance of L_3 is 10mH; Z_1 is formed by a 200Ω resistor connected in series with a 10mH inductor, which represents the domestic load of a residential home; and Z_2 is formed by a 5Ω resistor connected in serial with a 10mH inductor, which represents the public loads in a community. The grid voltage is a sinusoidal voltage of frequency 50 Hz.

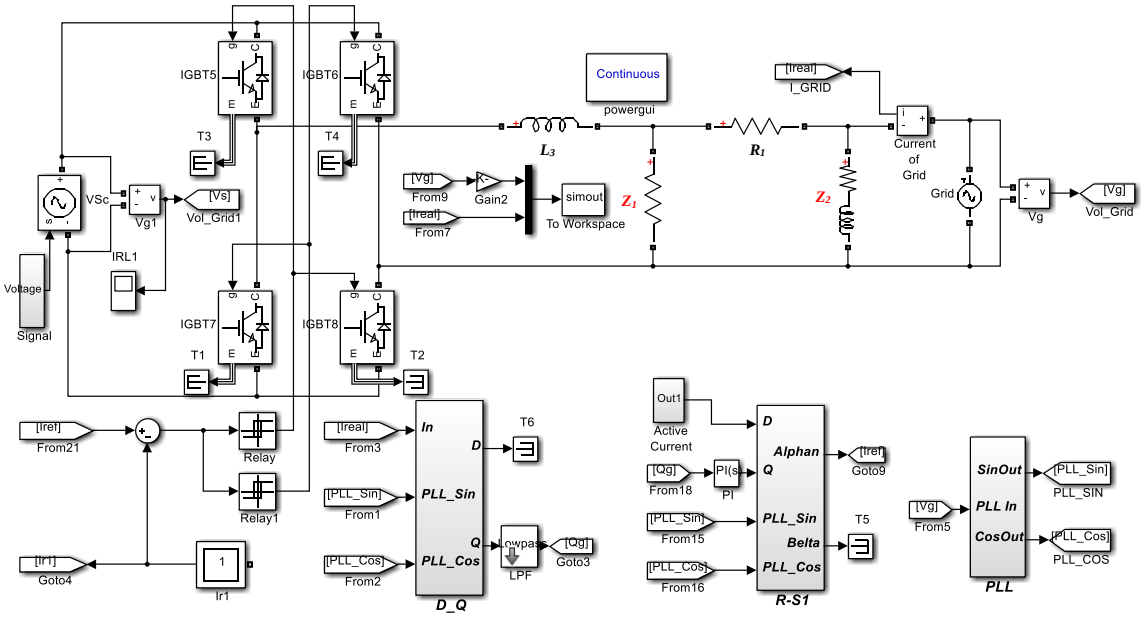


Figure 6- 15 Modelling of single-phase inverter

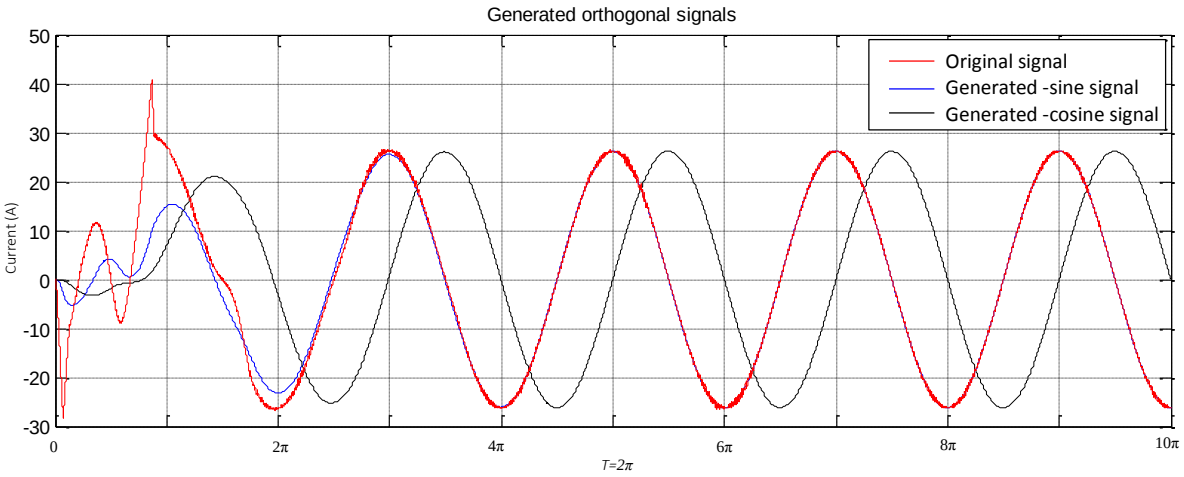


Figure 6- 16 Generated orthogonal signals

Figure 6-16 illustrates the simulation results of the orthogonal system output a pair of 50Hz negative sine (black trace) and negative cosine wave (blue trace) with respect to a 50Hz input negative cosine wave (red trace) signal. This figure shows that the two output sine (black trace) and cosine (blue trace) signals accurately formed a quadrature pair. Although there is some transient error when the system is started, the system rapidly reaches steady-state conditions (within one cycle) and the produced sinusoidal signal coincides with the input signal.

Constructing a pair of orthogonal signals is a foundation of splitting active and reactive current for single-phase system, so the simulation results mean that a pair of orthogonal signals have been successfully constructed for splitting active and reactive current in single-phase system which will be described in the subsequent section.

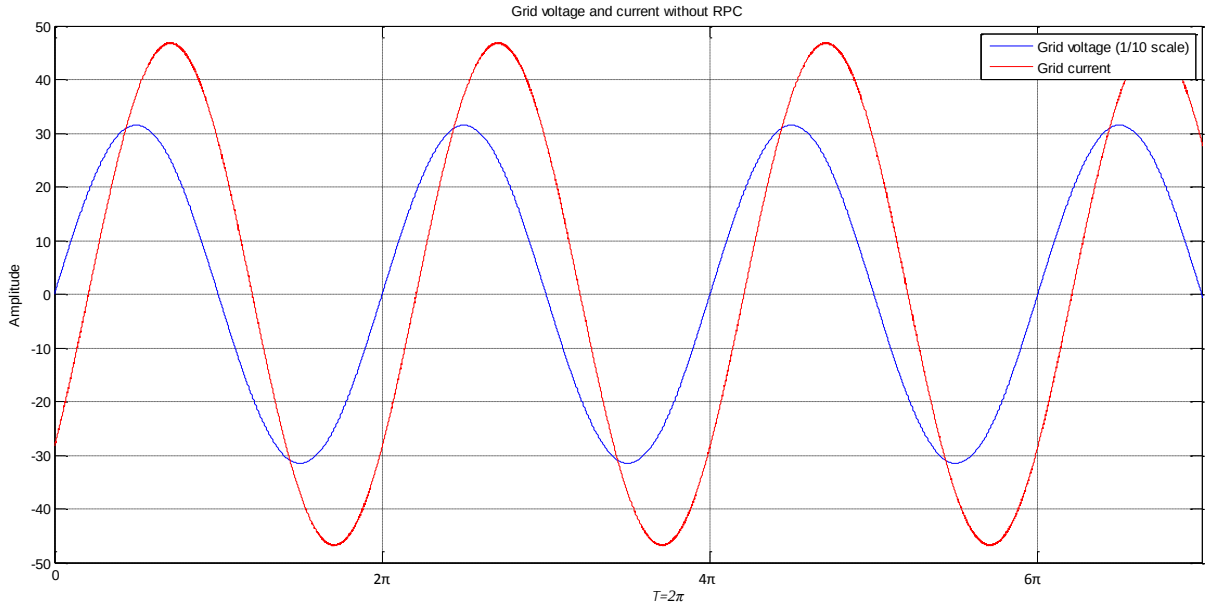


Figure 6- 17 Grid voltage and current without RPC

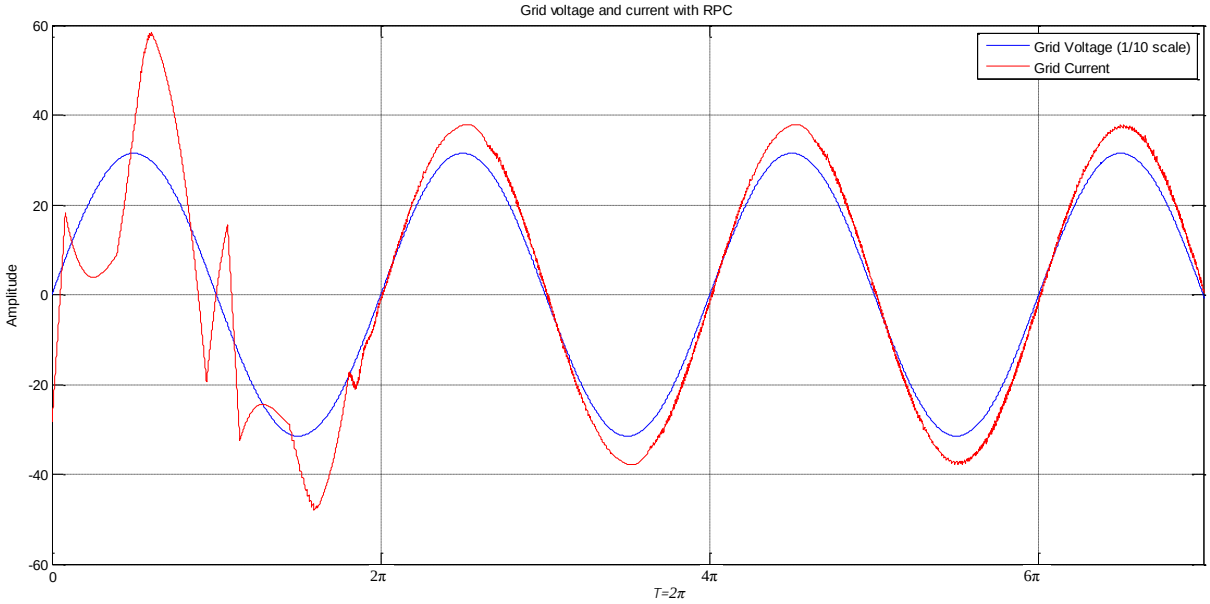


Figure 6- 18 Grid voltage and current with RPC

The load current lags the grid voltage by a certain phase angle, as shown in Figure 6-17. There is considerable contrast with Figure 6-18, in which, the phase angle of load current perfectly matches that of the grid voltage after RPC is applied to the grid by the inverter that utilizes the presented method of RPC.

Comparison of active and reactive power provided by the power grid before and after RPC is applied, and is illustrated in Figure 6-19 and 6-20 respectively. The results of simulation distinctly demonstrate that the reactive power supported by the grid has been dramatically reduced.

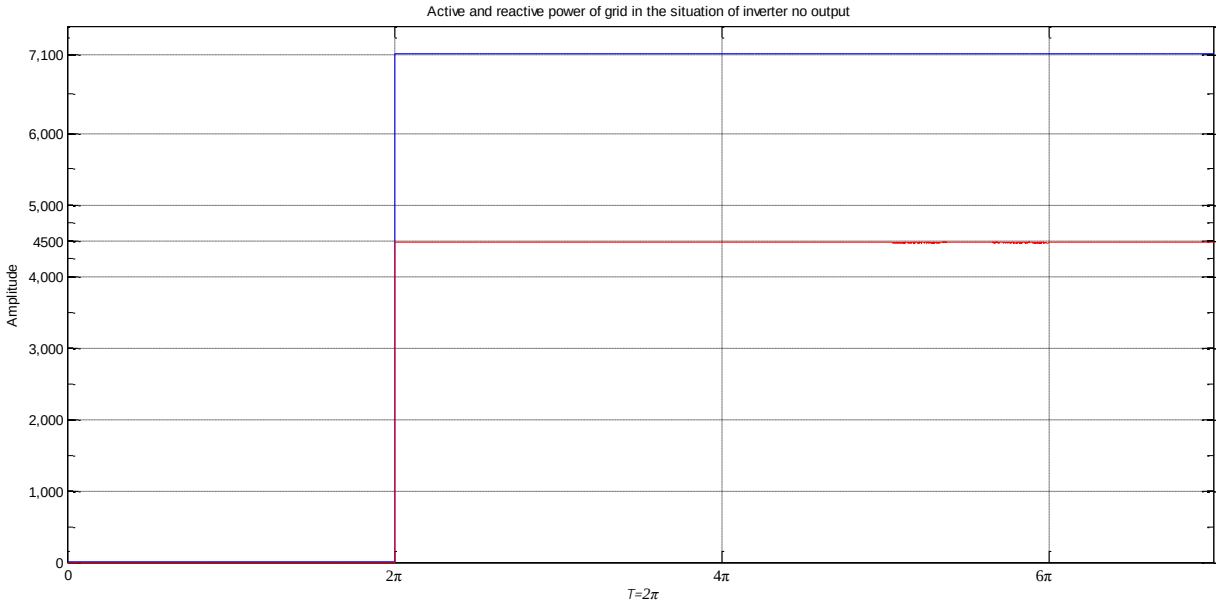


Figure 6- 19 Comparison of active and reactive power without RPC

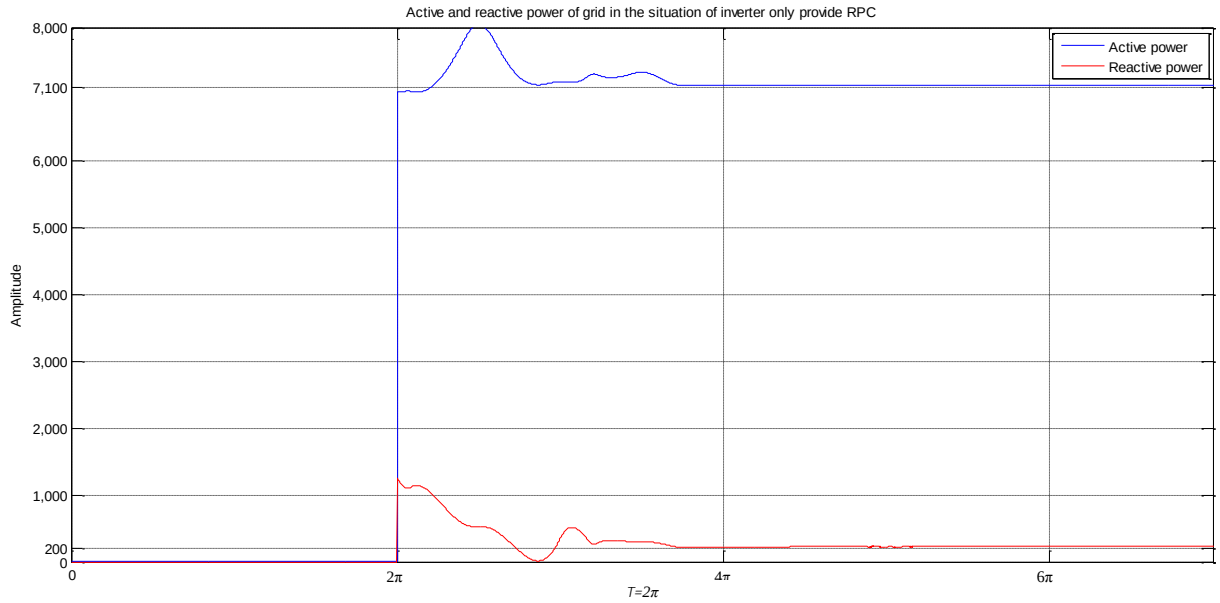


Figure 6- 20 Comparison of active and reactive power with RPC

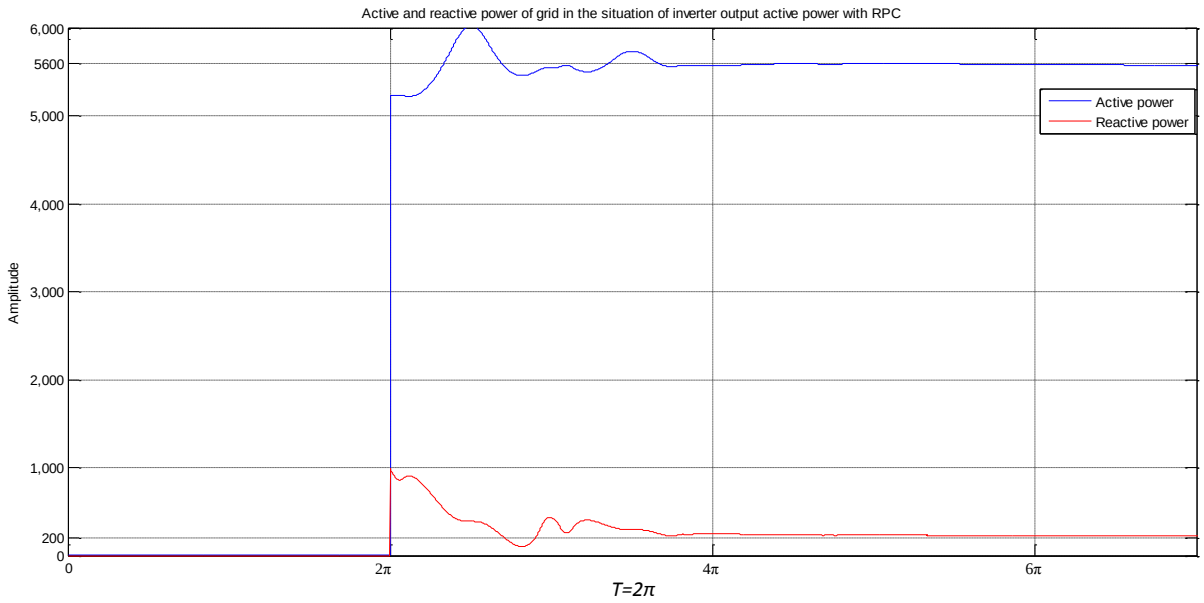


Figure 6- 21 Another comparison of active and reactive

Comparing Figure 6-20 and 6-21, the active power supported by the grid is reduced to approximately 5.8 kW in Figure 6-21 from previous 7.1 kW shown in Figure 6-20, whilst the reactive power provided by the grid in two Figures has not changed. This means that the simulation model of the GCI can quantitatively output active power and provide RPC. Therefore, it can also be said that the output of GCI can separately control the active power and reactive power according to the demands from the loads.

Figure 6-22 shows the simulation results of the GCI output without RPC. The red line shows that the inverter injects 0 power into the grid, from 0 to 4π. After 4π, the inverter starts to inject 8A into the grid. Figure 6-24 also demonstrates that the inverter will still provide power for the residential load when the inverter delivers 0 power into the grid (the green trace).

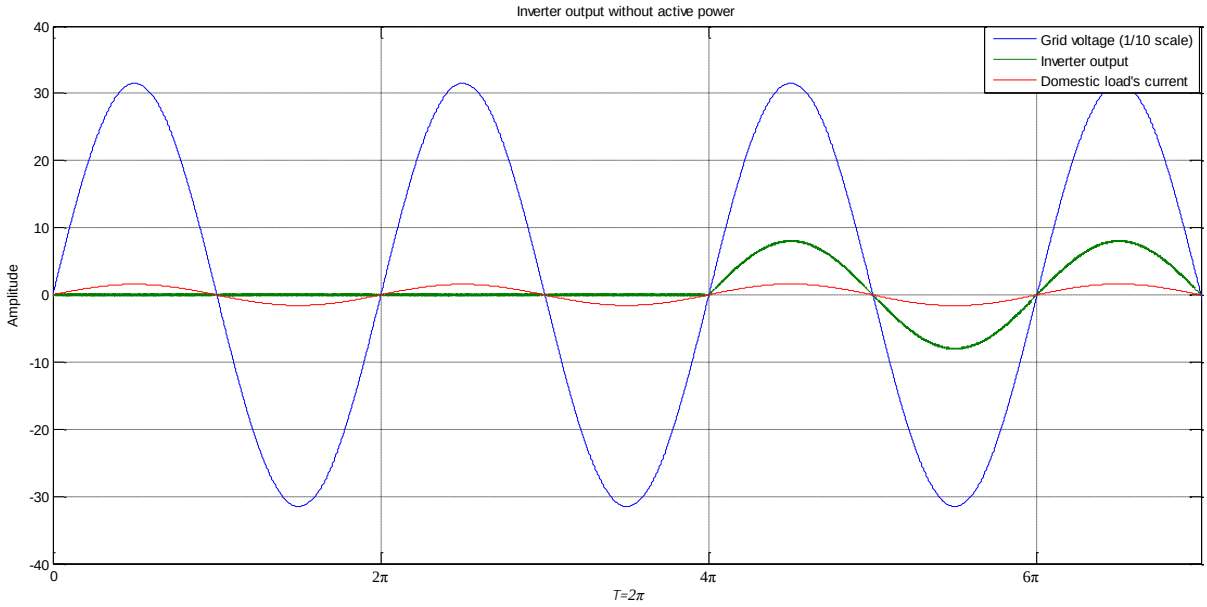


Figure 6- 22 Inverter injects zero power into the grid

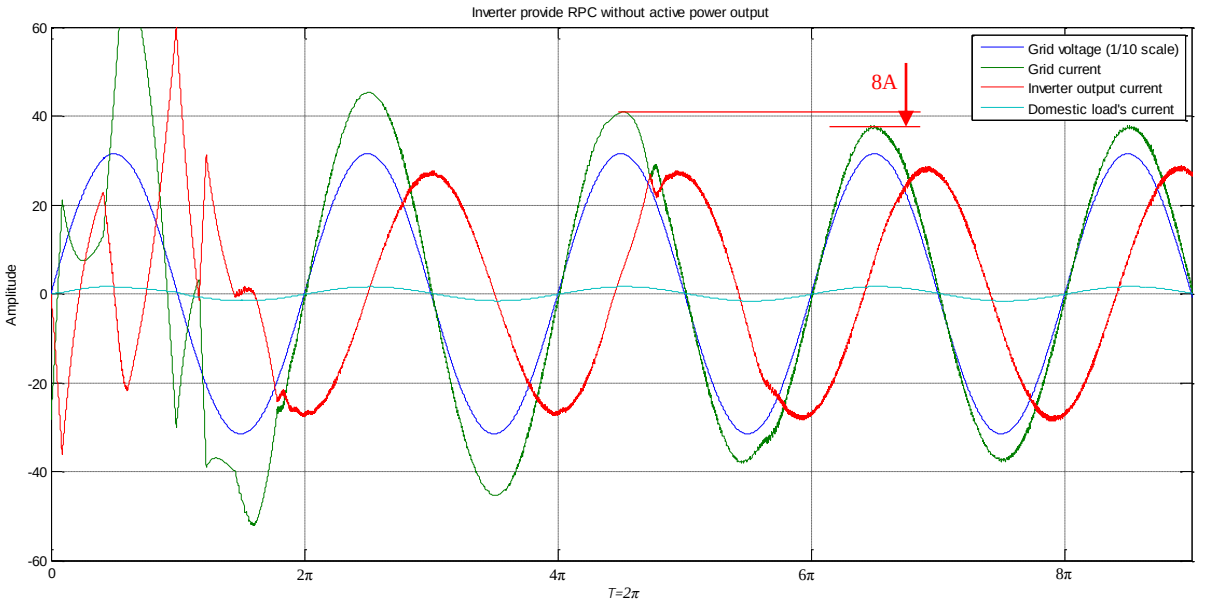


Figure 6- 23 Inverter injects zero active power with RPC

Figure 6-23 illustrates the simulation results of an inverter operating with RPC, but injecting 0 active power into the grid. The figure shows that the grid current (cyan trace) and the residential load current (green trace) are in phase with the grid voltage (blue trace). From 0 to 4π, the GCI only provides RPC for the load without injecting active power into the grid. After 4π, the inverter recovers to inject 8A active current into the grid. Therefore, after the inverter

has reached steady state conditions, the grid current reduces by approximately 8A comparing the peak values.

6.7 Simulation of three-phase GCI with RPC

In the previous section, the simulation of a single-phase GCI has demonstrated the feasibility of inverter output active power with RPC. In a whole community, one GCI being responsible for the reactive power requirement of the whole community is impossible. Figure 6-24 illustrates two three-phase GCIs connected with the power grid in parallel to jointly provide for the reactive power requirements of common facilities. The common facilities are formed by three resistor-inductor (RL) loads in star connection, each RL load consists of a 10Ω resistor connected in series with a 5mH inductor. The output filter of both inverters is formed by a 0.5Ω resistor connected in series with a 2mH inductor. For the simulation system, the input DC bus voltage is 600V, the peak value of the grid voltage is 310V and frequency of the grid is 50Hz.

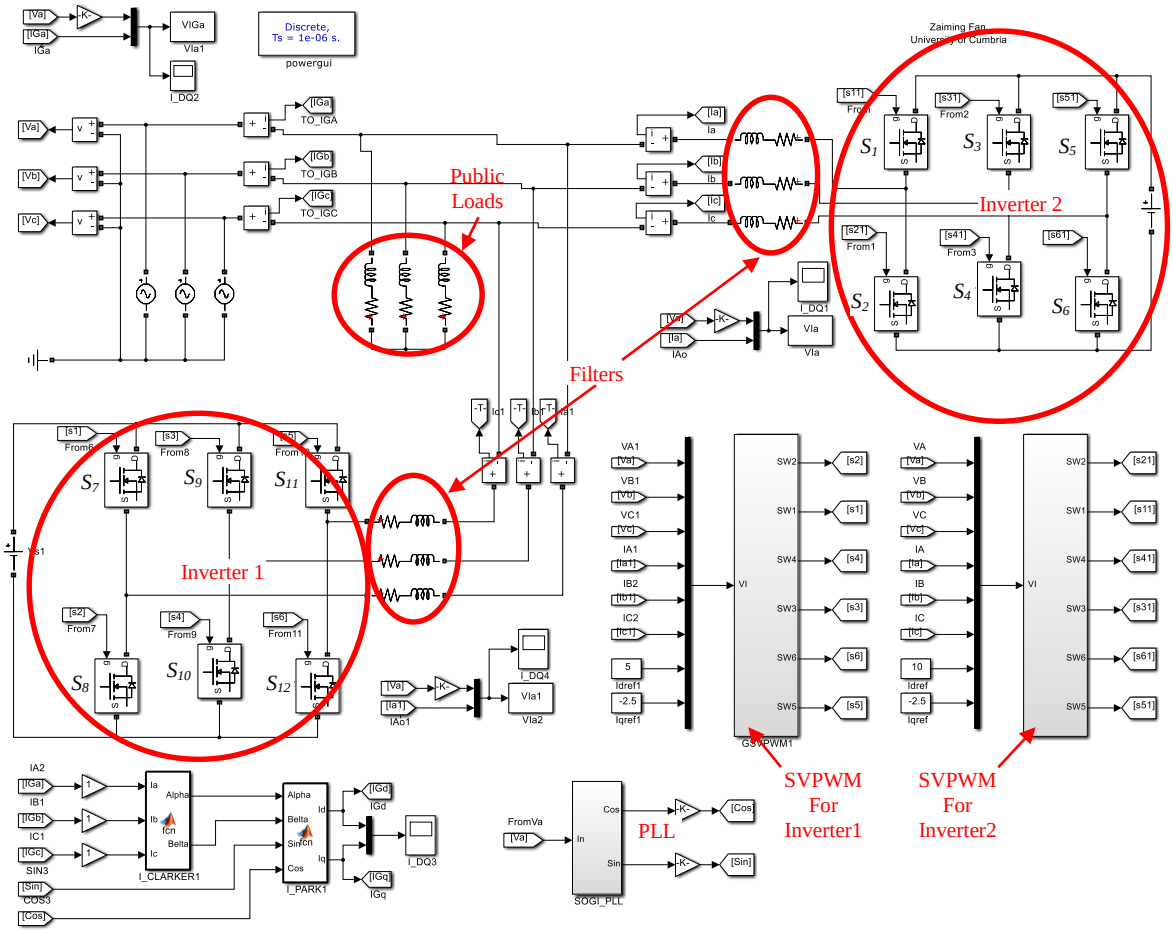


Figure 6- 24 Three-phase GCI with RPC

Simulation results of the current and voltage of Phase A of the three-phase GCI are shown in Figure 6-25. It is apparent that the grid current is in phase with the voltage, which means the reactive power requirement of common facilities has been compensated by the two inverters.

Figure 6-26 shows the Phase A currents of the two inverter outputs, the Phase A grid current and the Phase A voltage waveforms. Although the two inverter output currents are not in phase with each other and not the same amplitude, the grid current is in phase with the voltage.

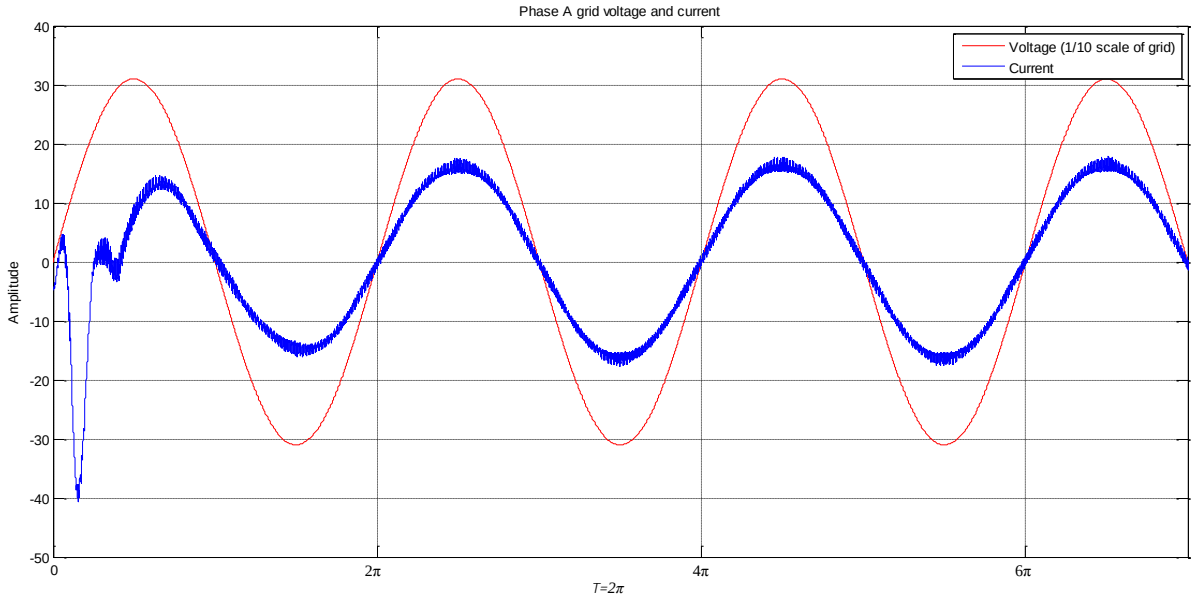


Figure 6- 25 Current and voltage of the gird

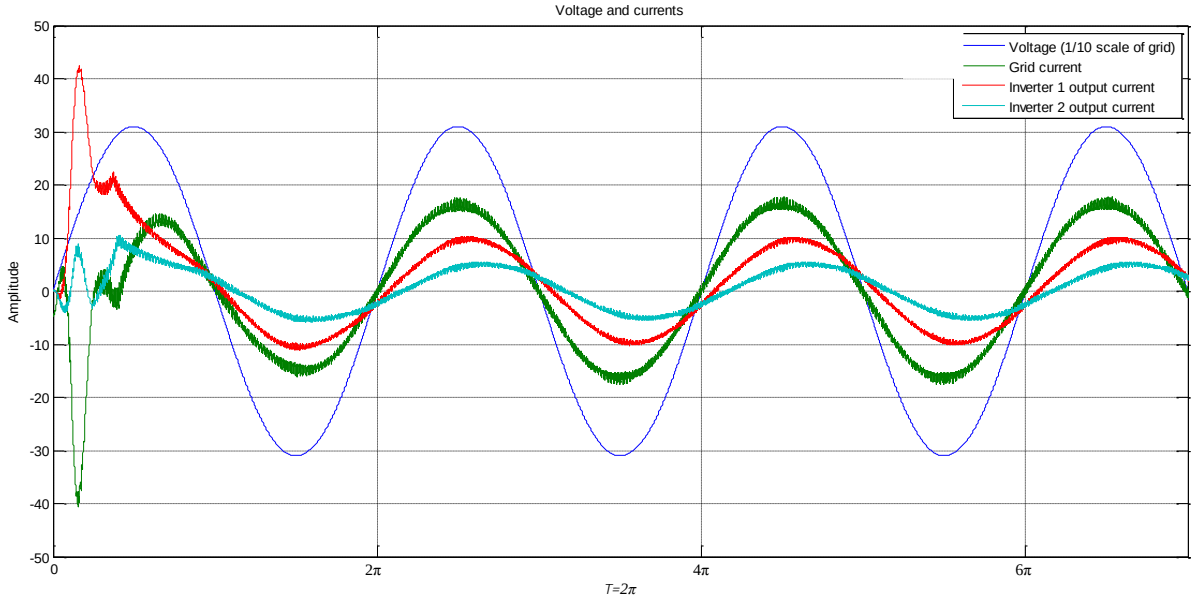


Figure 6- 26 Current and voltage waveforms

6.8 Modelling of multi-inverter with RPC

Figure 6-27 shows the MATLAB/Simulink model of three GCIs forming a small scale distributed generation system, which supplies power to a community. In the simulation model, the three inverters can be considered as 3-5kW individual GCIs, for individual resident homes

delivering power to the micro-grid, and controlled by a central controller. R_3 represents public facilities (such as small-scale wind turbine, any equipment contained motor, transformer.), which is formed by a 5Ω resistor connected in series with a 10mH inductor. R_2, R_6 and R_7 represent domestic loads which are 200Ω. R_1, R_4 and R_5 represent the equivalent impedance of filter inductors and distribution lines, which are 10mH.

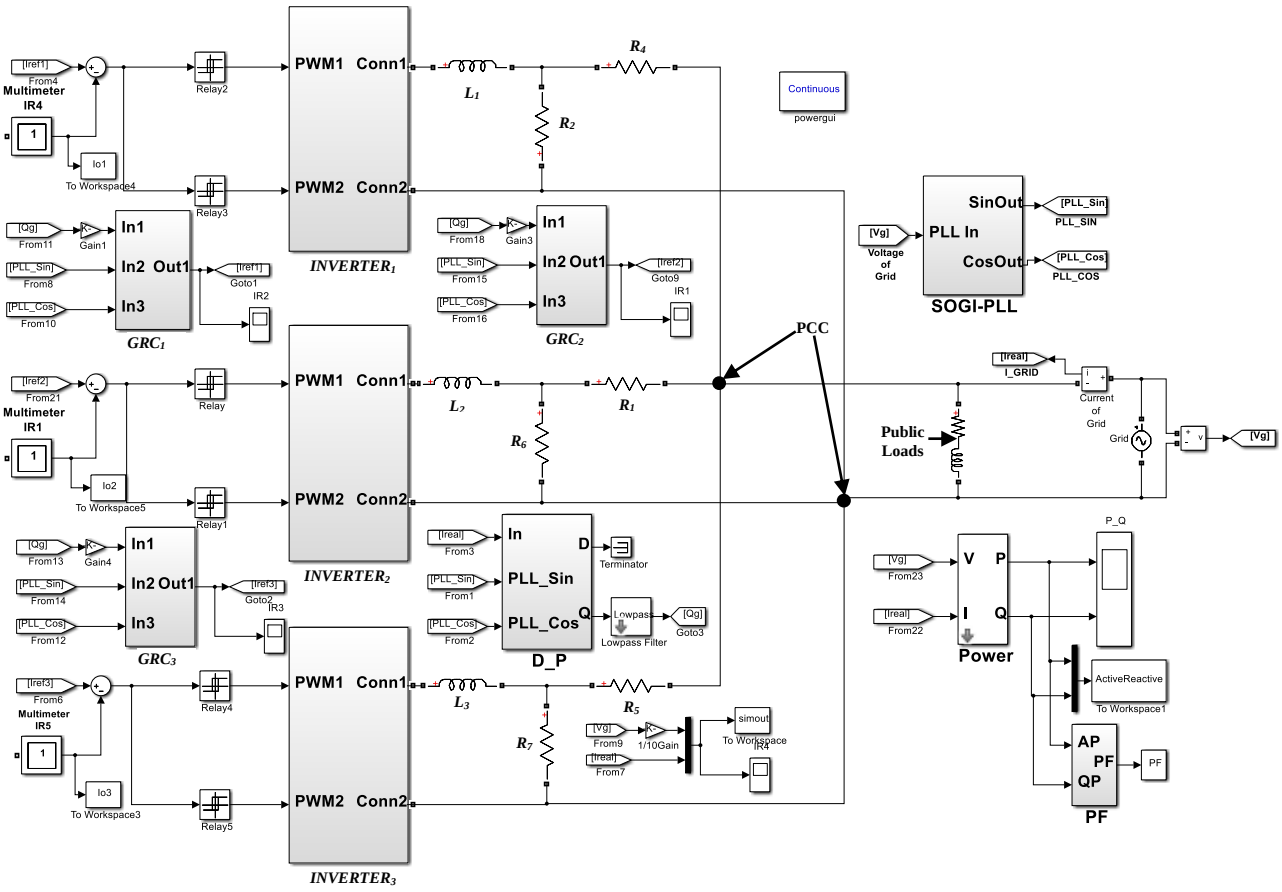


Figure 6- 27 Multi-inverters with RPC in a micro-grid

In Figure 6-27, the D_P block separates active and reactive current of the grid, the blocks of GRC_1, GRC_2 and GRC_3 generate reference currents for each inverter with respect to the demanding active and reactive current. In the simulation model, $INVERTER_1$ provides 4A of active power current with 1/3 of the reactive power current of the public facilities for the micro-grid, $INVERTER_2$ delivers 8A of active power current with 1/6 of the reactive power current of

the public facilities for the micro-grid and $INVERTER_3$ generates 10A of active power current with ½ of the reactive power current of the public facilities for the micro-grid.

Figure 6-28 illustrates the simulation results of the grid current and voltage; the grid current is in phase with the voltage with the three inverters sharing reactive power. Figure 6-31 demonstrates that the simulated power factor of the grid at the PCC is extremely close to unity, which means the required reactive power of public facility in the micro-grid has been compensated collectively by the three distributed GCIs.

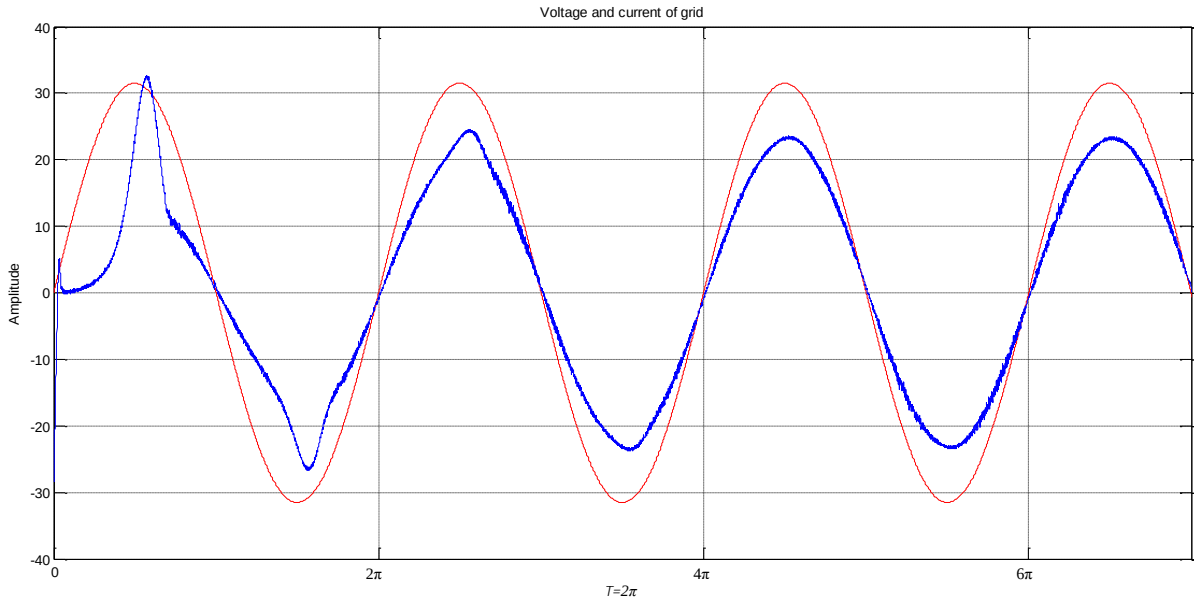


Figure 6- 28 Current and voltage of the gird

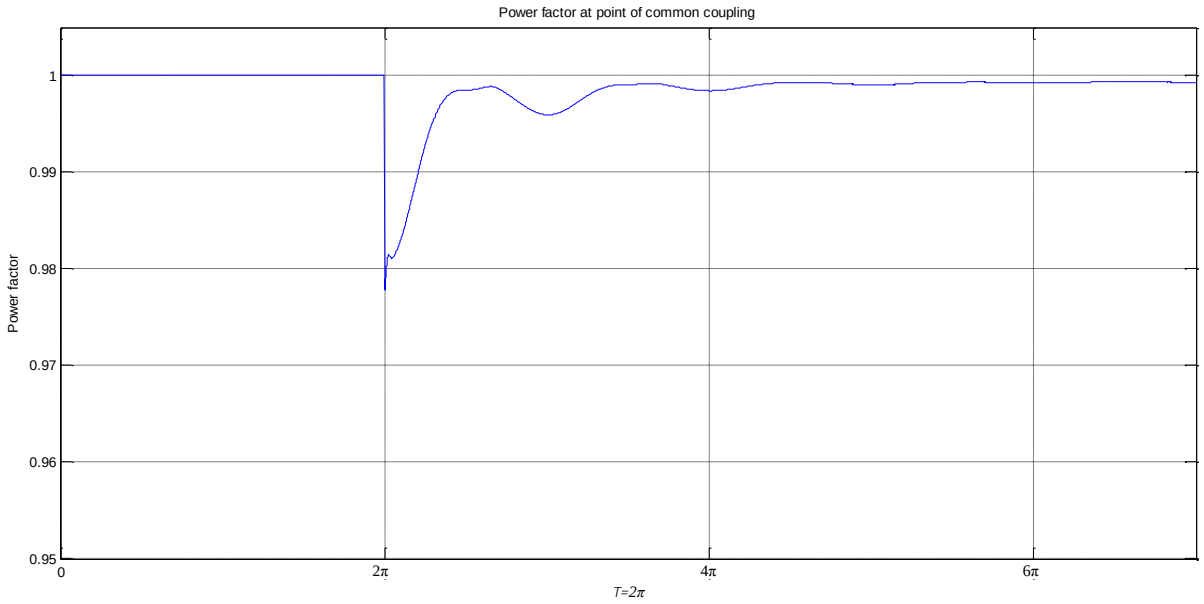


Figure 6- 29 Power factor

Figure 6-30 shows the output currents of the inverters, the grid current and the grid voltage. It is clear that inverter output currents are neither in phase with each other nor the grid voltage, and the amplitudes of the inverter output currents are not equal. However, the grid current is completely in phase with grid voltage. This demonstrates that each GCI can supply different amounts of active and reactive power according to its own circumstances.

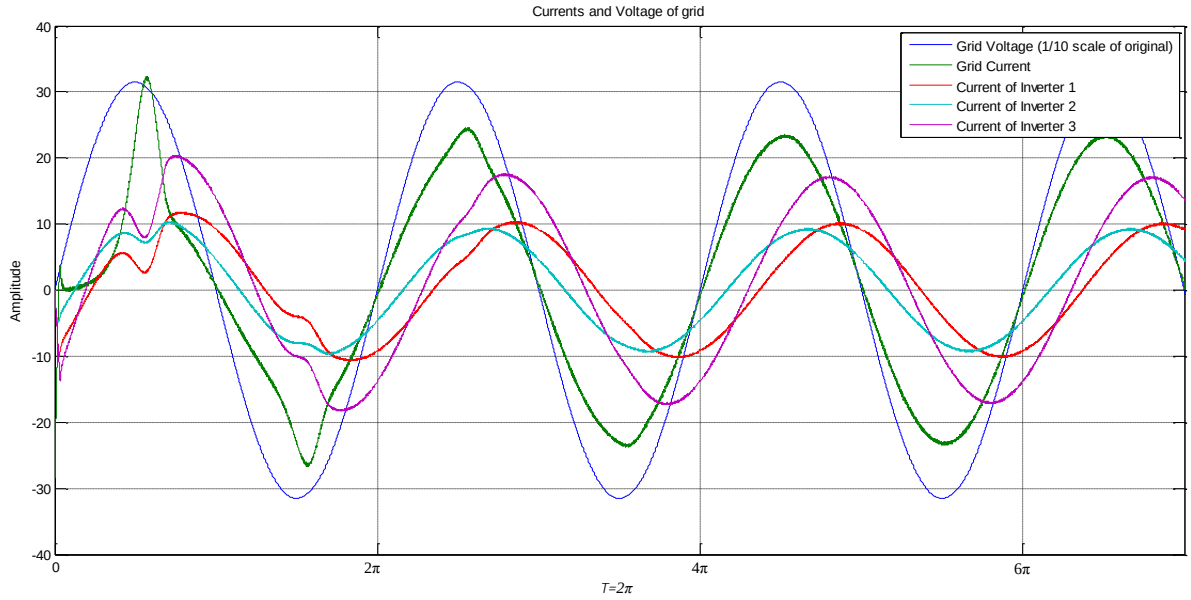


Figure 6- 30 Currents and voltage after PFC

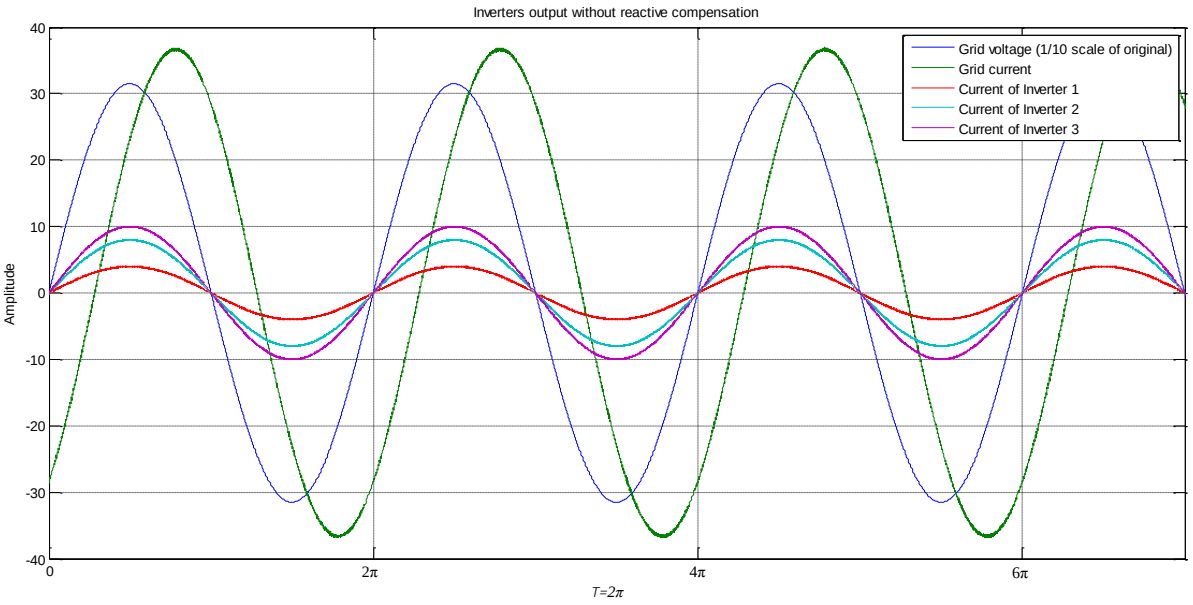


Figure 6- 31 Conventional inverter output current and grid voltage

Figure 6-31 illustrates the output current of three inverters when they only inject active power into the grid, in which, the output current of the inverters are in phase with the grid, but the grid current increases approximately to 12A comparing with Figure 6-30.

6.9 Experimental verification of off-grid inverters

Ensuring that the output voltage of a GCI is synchronised with the grid voltage is a fundamental prerequisite, which allows the inverter to be connected to the grid. As the result of a collapse of the grid, which happens occasionally (due to for example load shading, feed transformer failure), all the inverters installed in a community will be turned off due to the loss of the synchronising signal. Therefore, it is necessary to provide a synchronising signal for all the inverters in the micro-grid system to ensure them working on off-grid mode properly without support from external frequency and phase signals from the grid, such as through a diesel generator. It is very complicated to enable an inverter to perform the function of a synchronous generator (Zhong & Hornik, 2013). In a practical smart micro-grid, an uninterruptible power supply (UPS) is usually installed at the circuit breaker, which is adapted to interface with the

grid to provide a synchronising signal for all the inverters in the micro-grid community. Zero-crossing method is the simplest way to yield the grid frequency and phase angle information (Gardner, 2005). This section proposes a novel method to generate a small zero-crossing signal by the central controller in a practical application to enable the inverters in a micro-grid to operate properly on off-grid mode.

6.9.1 Generating synchronous signal

An ARM7 core LPC2132 from NXP is utilised to generate the synchronising signal. In the experimental set-up, a case study of an inverter output voltage of frequency 50Hz is considered. Therefore, the central controller only needs to generate a square wave of 50Hz with 50% duty ratio for all the inverters.

Assuming a 50Hz sinusoidal wave has 256 sampling points, i.e. the time interval between each sampling point is 1/50/256 = 78.125us. The external crystal of ARM LPC2132 is 11.0592 MHz, the internal core clock frequency is configured as 5 times the external crystal frequency and the clock frequency of ARM peripheral bus is half of internal core clock frequency.

Figure 6-32 shows that the Timer 0 block in the LPC2132 connects with ARM peripheral bus, the number of clocks cycles between each sampling point can be obtained as follows:

$$N_c = \frac{F_{pclk}}{2F_g N_s} \qquad (6-11)$$

where

N_c is the number of clock cycles between each sampling point

F_{pclk} is the frequency of ARM peripheral bus

F_g is the frequency of electrical power

N_s is the number of sampling point in each period.

Therefore, if the value of Prescale Register 0 T_0PR in LPC2132 is configured to be N_s, and the Match Register 0 T_0MR_0 is configured as 1, when the Timer 0 Counter T_0TC is equal to T_0MR_0, Timer 0 interrupt can be triggered automatically to produce a toggle of one of the input and output (IO) pins as an output in the Timer 0 interrupts routine to broadcast a synchronising signal for each inverter.

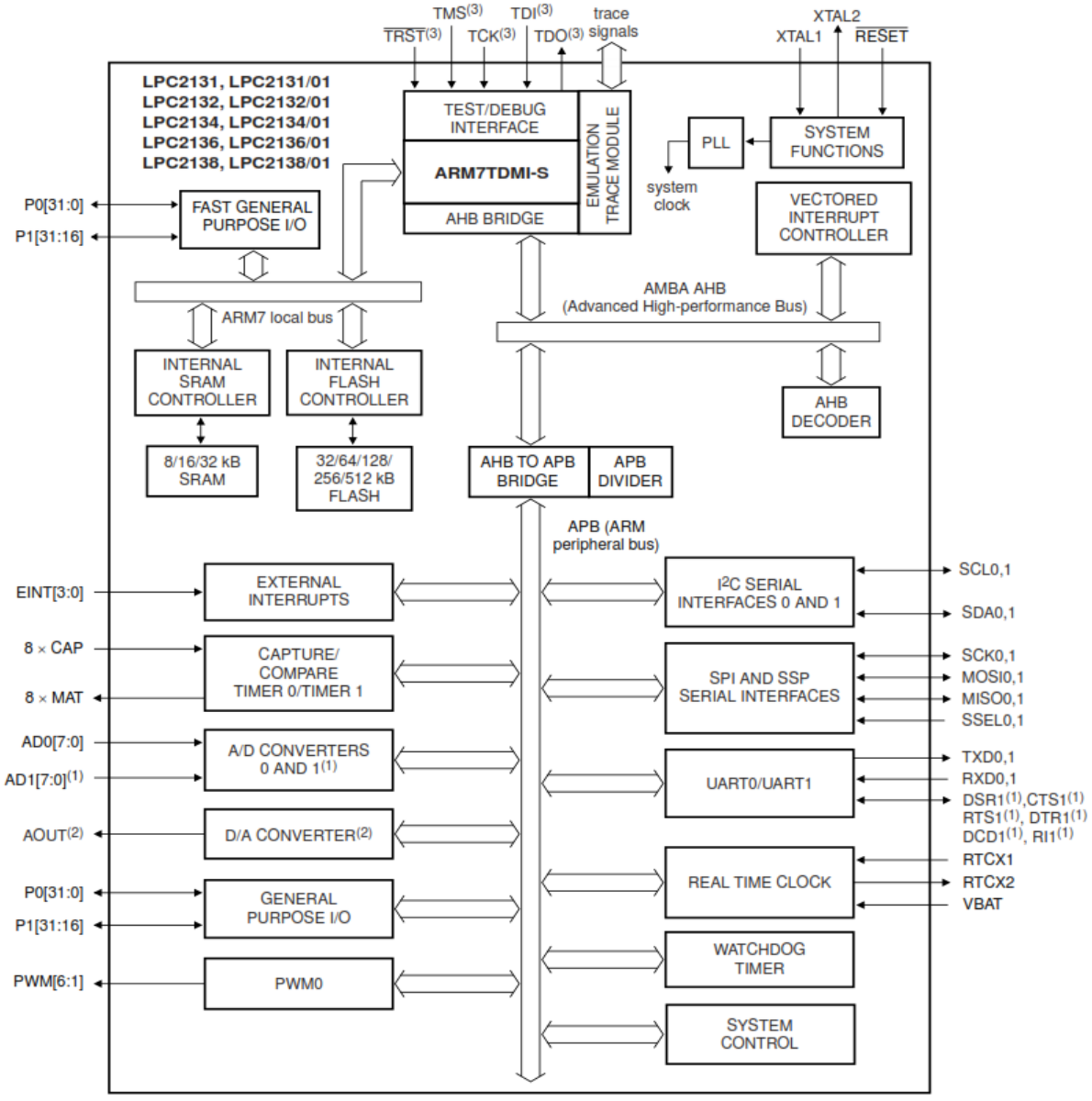


Figure 6- 32 LPC213x block diagram

Taken from (NXP Semiconductors, 2012)

6.9.2 Frequency synchronisation

Figure 6-33 illustrates a square wave with 50% duty ratio; the conventional approach starts counting clocks at the rising at point A, storing the number of clock cycles at the falling edge at point B and stopping the count and storing the number of clock cycles at point C, then calculates the total number of clock cycles captured over one cycle, which can be used to determine the frequency of the square wave.

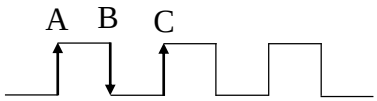


Figure 6- 33 Square wave

Signal attenuation in a practical long-distance transmission system is a concern. This can result in inaccurate determination of the frequency. The key parameters of the inverters' output frequency and number of samples can be broadcasted to all inverters through communication by the central controller. Then, each inverter starts from 0, counts to the sampling number and each rising edge resets the sampling sequence to 0.

6.9.3 Experiment and results

Figure 6-34 shows a lab simulation model of smart micro-grid comprising three 1kW C2000 solar DC/AC Single-Phase Inverters working at off-grid mode; an ARM LPC 2132 development toolkit board which is employed to represent the central controller to generate the synchronising signal for three inverters. 110 MHz digital storage oscilloscope with two input channel was used to measure inverter and control centre output signals. Programming IDE is based on ARM MDK, using the joint test action group (JTAG) simulated tool to debug and download program.

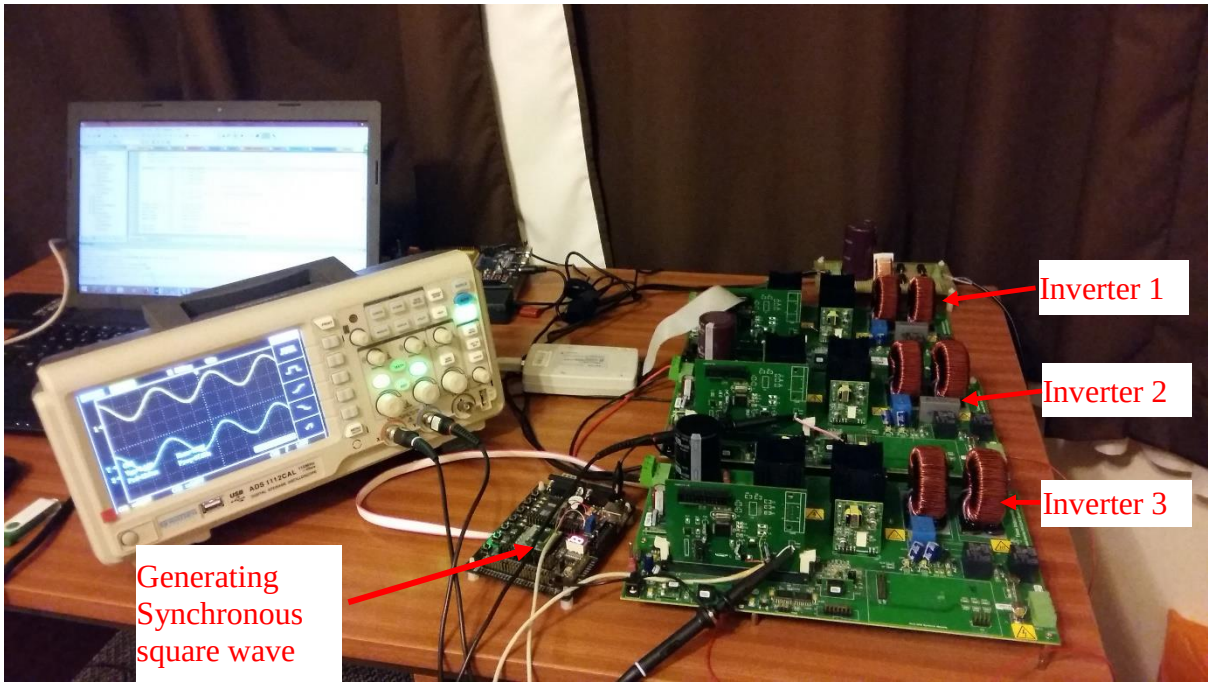
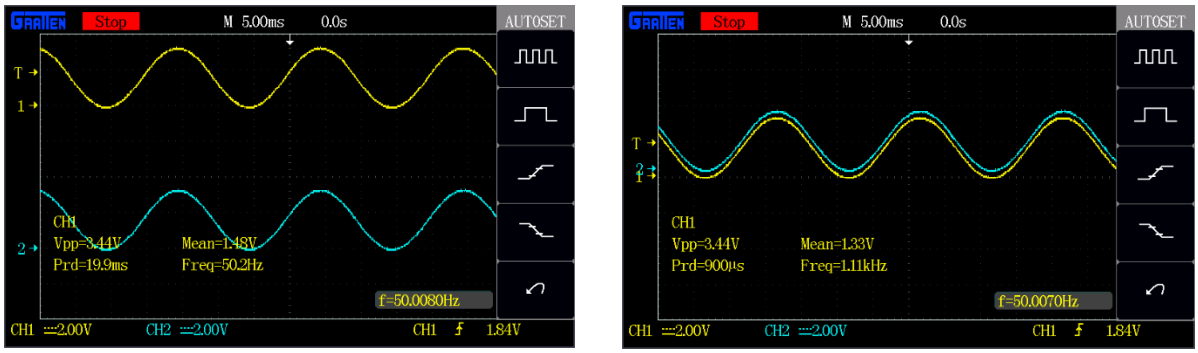


Figure 6- 34 Experimental setup of three off-grid inverters connected togother

Figure 6-35 (a) illustrates the output results of inverter$_1$ (Yellow trace) and inverter$_2$ (Cyan trace), 6-35 (b) shows the output results of inverter$_2$ (Cyan trace) and inverter$_3$ (Yellow trace). The results in Figure 6-35 clearly demonstrates that the output voltages of the three inverters are completely in phase with each other.



(a) Output of inverter1 and inverter2 **(b) Output of inverter2 and inverter3**

Figure 6- 35 Output voltages of two off-grid inverters

Figure 6-36 reveals the frequency of the inverter$_2$ (Cyan trace) output voltage, which synchronises with the input square wave which is shown in Figure 6-36 (yellow trace).

Considering Figures 6-35 and 6-36, it can be stated that the outputs of the three off-grid inverters are completely synchronised.

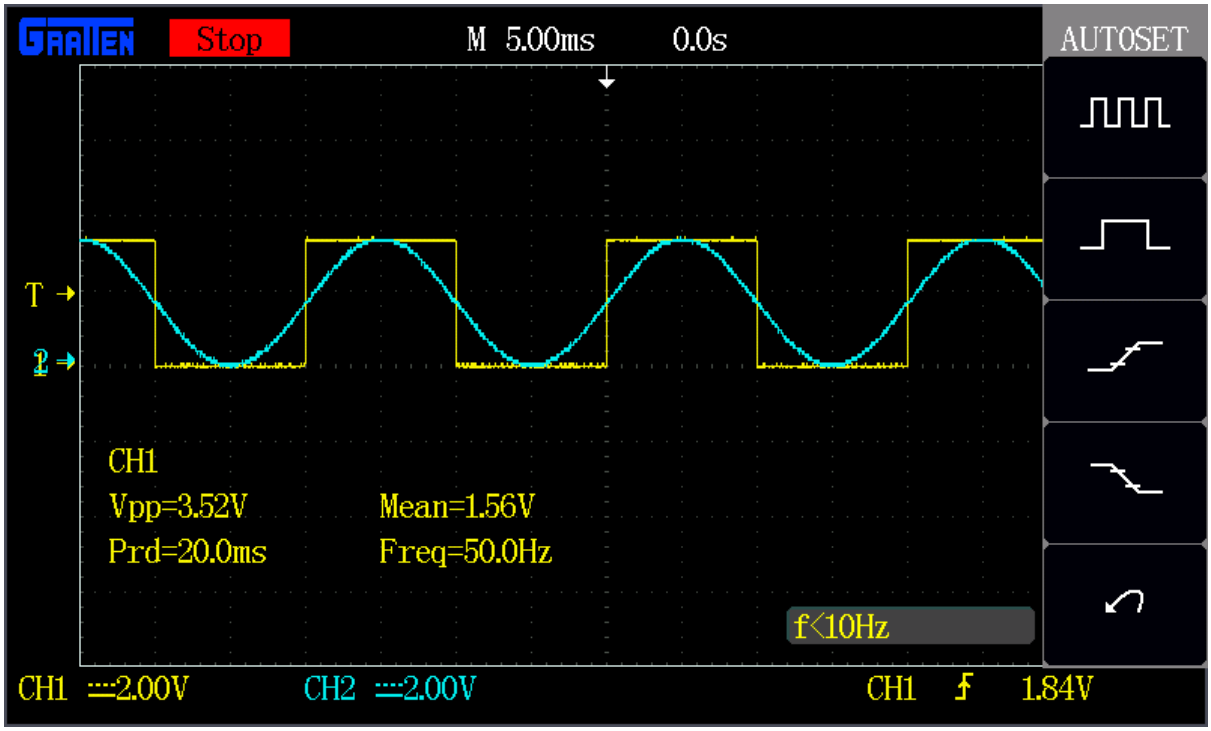


Figure 6- 36 Comparison of inverter output (Cyan trace) and input (Yellow trace) synchronous signal

6.10 Summary

Through modelling a GCI with RPC and analysing the simulation results, it has been demonstrated that the presented method of separating active and reactive current components of the grid to quantitatively control reactive power has been successfully achieved. That means the inverter can inject controlled active power into the grid and provide certain amounts of RPC. It has also been demonstrated that the inverter can inject zero active power into the grid and operate as STACOM providing RPC for the grid. In Section 6.9, the comparison of experimental results from the three off-grid single-phase inverters has shown that they can be synchronised whilst working on off-grid mode in a community micro-grid.

Chapter 7 Conclusions and Future Work

7.1 Conclusions and Discussion

This project implemented a simulation model of a smart micro-grid in which RPC was achieved through each GCI in the smart micro-grid by quantitatively producing a certain amount of reactive current so as to collectively share the reactive power demand from the smart micro-grid. A bi-directional DC/AC inverter and an interleaved DC/DC converter was simulated in MATLAB/Simulink, which was employed to charging and discharging battery storage. In experimental work, implemented three-phase SVPWM rectifier based on a full-bridge inverter circuit. Another experimental work connecting three 1kW inverters to simulate a small-scale micro-grid demonstrated that anyone of inverter output voltage and phase is consistent with each other's without support from external grid voltage, frequency and phase signals, typically from a diesel generator. The significance of solving the issue of synchronisation of the inverters in a micro-grid is that domestic users are not seriously affected in the event of grid collapse or cut off, or the micro-grid working in standalone mode.

In order to provide the micro-grid with a stable and continue power supply, the smart micro-grid not only operates under on-grid mode but also runs on off-grid mode.

There are a number of issues to be considered as the micro-grid works on off-grid mode, such as inverter synchronisation with the grid, RPC, remote control, optimisation and end-user's benefit. Except synchronous issue between the each inverter, all the issues addressed above have to be faced in GCI system as well. Therefore, detecting zero-crossing method implemented to allows three GCIs to be synchronised and work properly to solve inverter no power output in the situation of power cut-off while the generated sources are abundant.

An inverter and rectifier, based on the same IGBT full-bridge topology (let's call it as converter), has been successfully modelled in MATLAB/Simulink. The operating mode of the converter can be switched between inverting and rectifying modes in accordance with end-user's demands or by remote control. During low grid electricity tariff periods the converter may work as a rectifier taking electricity from the AC grid and storing DC power in a battery bank configured to enhance users' profit. When the converter operates in inverting mode the priority is to meet the residential demand on electricity, and only the excess power from the renewable power generator is injected into the power grid, which improves users' benefits and reduces reverse power flow to the power grid.

A single-phase GCI with RPC and rectifier input PFC has been developed, adopting the same algorithm employed in three-phase GCI to separate the active and reactive power for the inverter output. This reduces code and data size, increases code execution speed and saves memory space in practical application real-time system.

Chapter 4 presented detailed step-by-step design procedures and simulation of a SOGIPLL for a real-time system. Simulation results demonstrate that the SOGIPLL algorithm has strong anti-interference performance.

Chapter 5 introduced a topology of a four-phase IBDBBC to implement a bi-directional DC power transfer between a low voltage battery storage system and a high voltage DC bus. Simulation results reveal that the ripple voltage of the converter output was significantly reduced, which allows the size of the filter elements to be reduced, and the power switching device's voltage and current stresses have been significantly improved. However, the cost of the four-phase IBDBBC was higher than the cost of a simple circuit topology.

Chapter 6 presented a lab simulation model of a micro-grid comprising three shunt GCIs. In the lab simulation model, the three inverters inject different amounts of active power into the

grid and provide different amounts of reactive power for common loads to successfully implement RPC for the micro-grid.

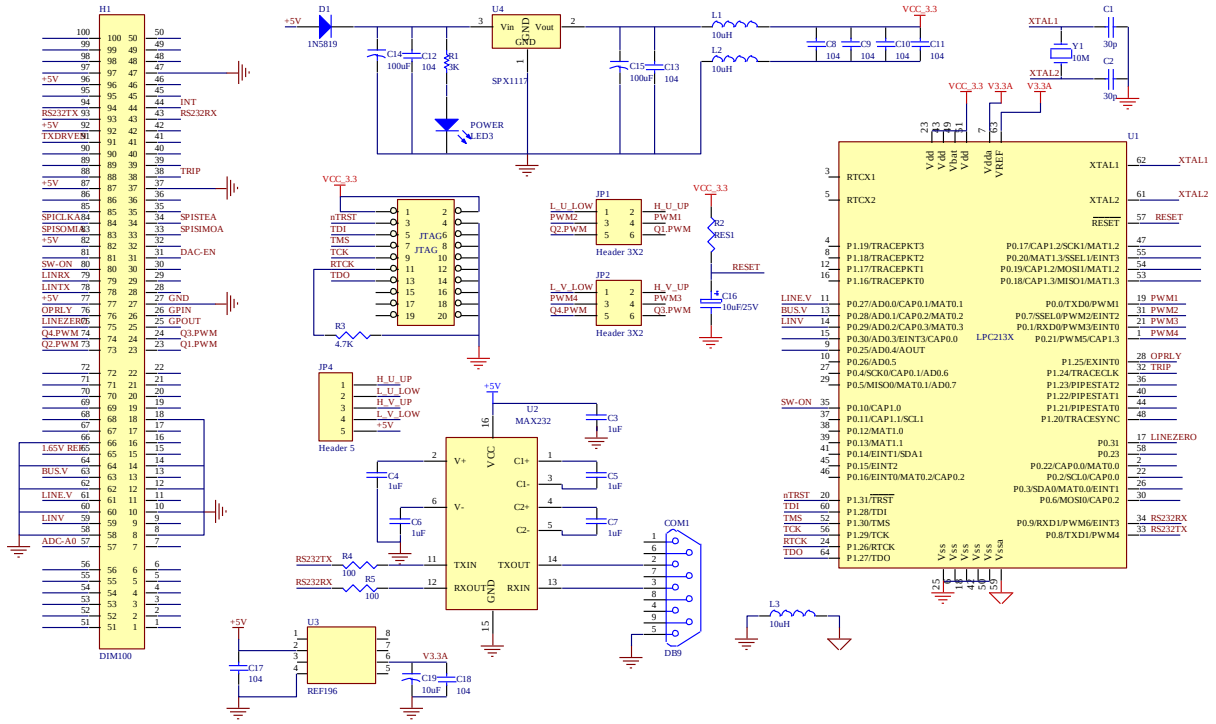
7.2 Future work

Although the three-phase GCI and the four-phase IBDBBC have been designed and modelled in MATLAB/Simulink, it was not implemented in a practical application due to limited lab resources.

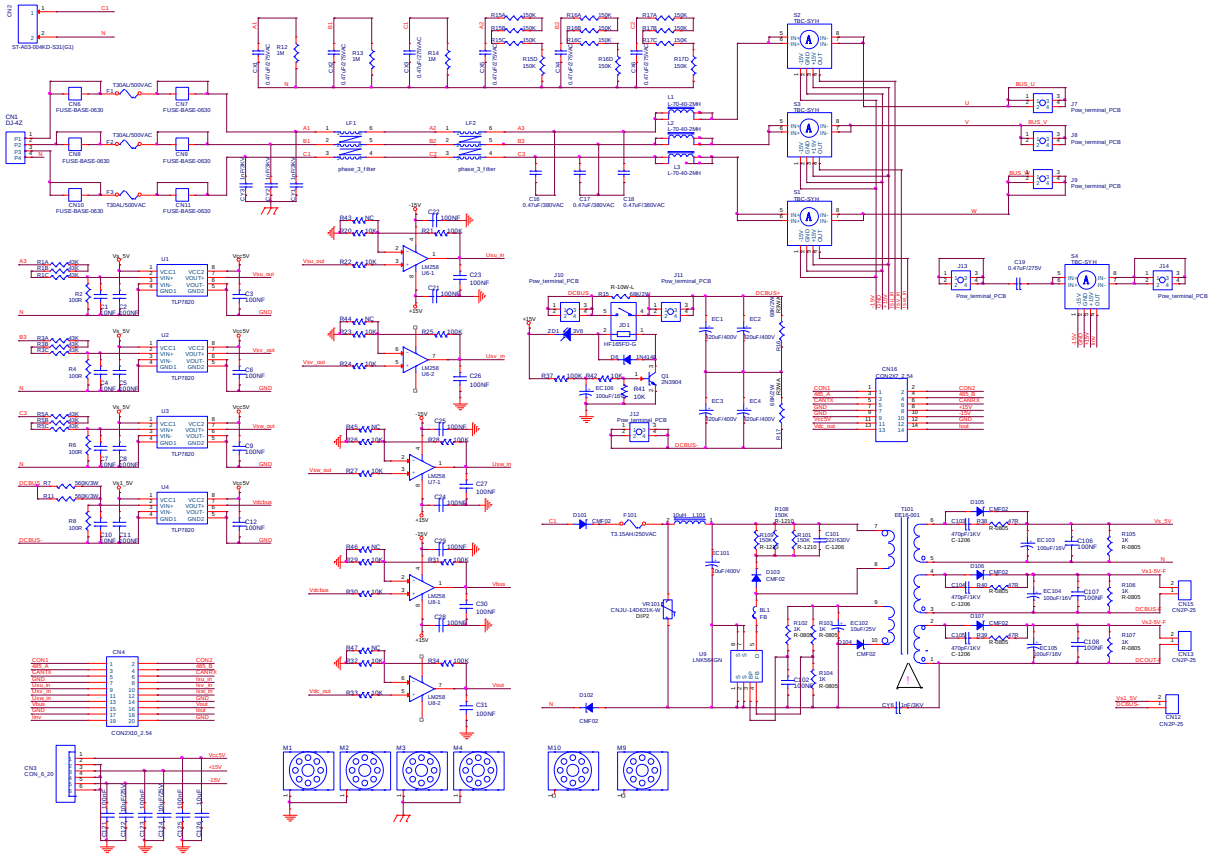
Theoretical analysis reveals that a change of reactive power demand will be reflected in a change in voltage at the side of inverter output . However, in a practical application, due to the intrinsic voltage fluctuations and harmonics on the power grid, measuring the voltage change to derive the RPC is very difficult. Further work is needed to overcome these problems and thereby improve the RPC in real systems.

This project and thesis have focused only on the core technology of implementing the functionality of a micro-grid system. It was impossible to consider the battery storage system in terms of capacity, configuration and lifecycle. Those factors need to be investigated in the future to determine the optimum battery storage system solutions suitable for end-users with different generation potential and residential loads, whilst also considering storage system costs, power sourcing and grid electricity tariff.

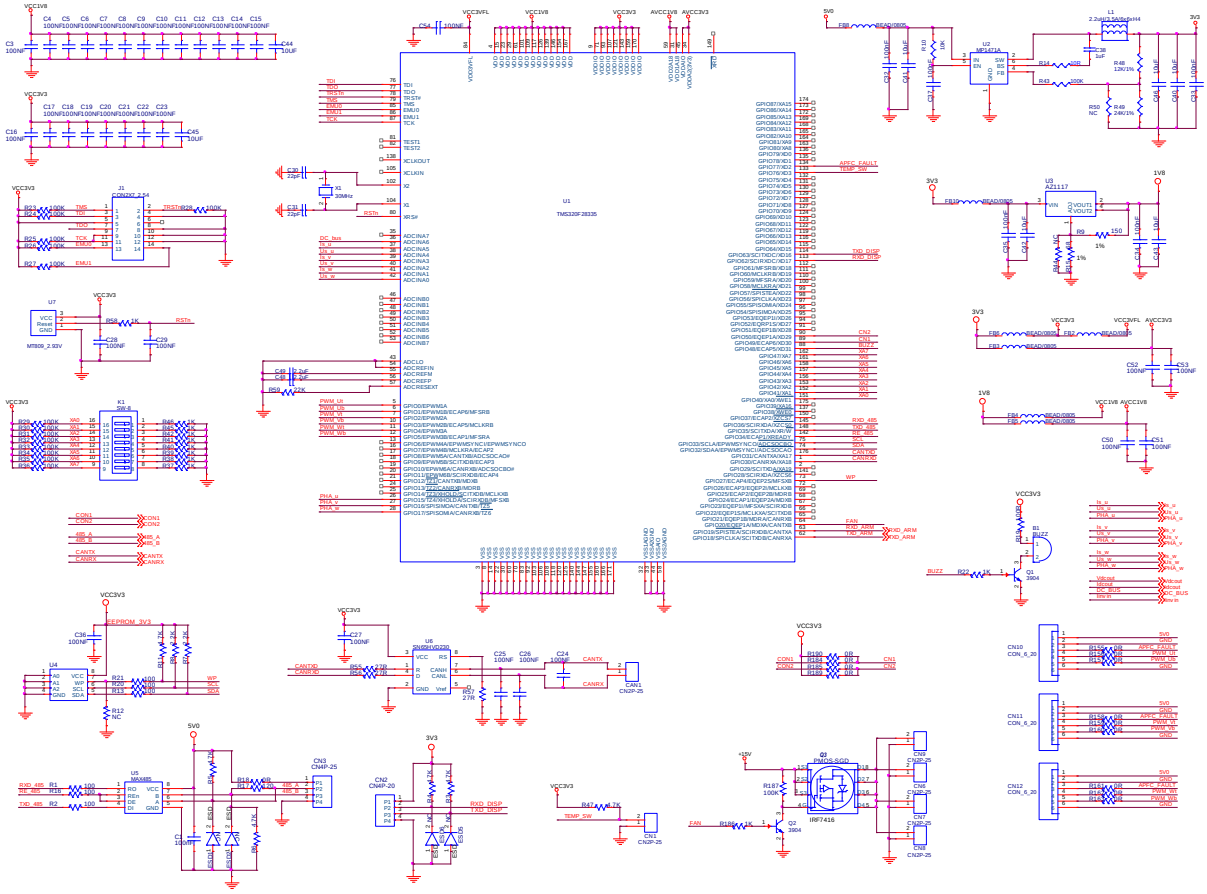
Appendix A Schematic Of Control Board For Single-Phase Inverter



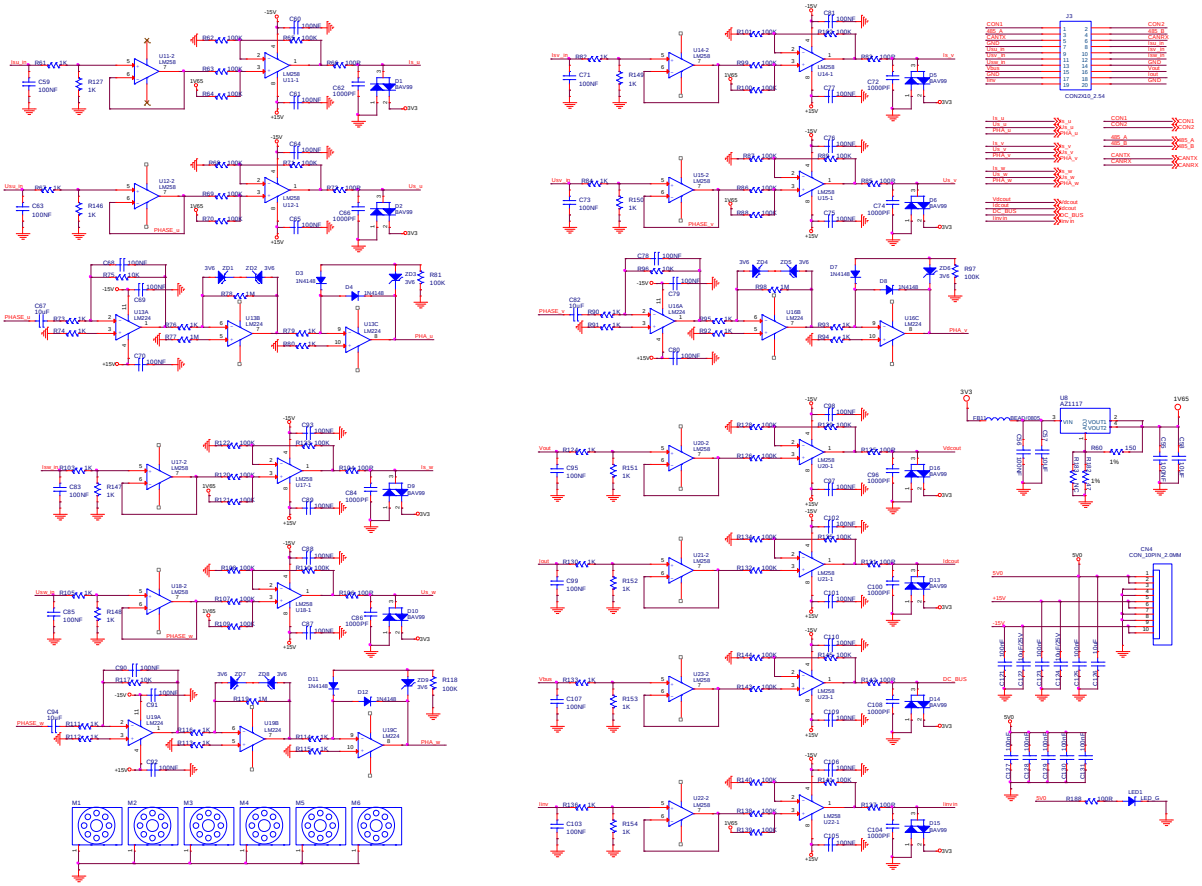
Appendix B Schematic Of Sensors



Appendix C Schematic Of Main Control For Rectifier



Appendix D Schematic Of Signal Pre-Processing



Appendix E MATLAB Function Program

E.1 Clarke's transformation

```
function [Alpha,Belta]= fcn(Va,Vb,Vc)
%#codegen
Alpha = 2*(Va-(Vb+Vc)/2)/3;
Belta = 1.732*(Vb-Vc)/3;
```

E.2 Park's transformation

```
function [Vd,Vq]= fcn(Alpha,Belta,Sin,Cos)
%#codege
Vd = Alpha*Cos + Belta*Sin;
Vq = Belta*Cos - Alpha*Sin;
```

E.3 Inverse Park's transformation

```
function [Alpha,Belta]= fcn(Vd,Vq,Sin,Cos)
%#codege
Alpha = Vd*Cos - Vq*Sin;
Belta = Vq*Cos + Vd*Sin;
```

E.4 Identify area

```
function [Area,T1,T2]= fcn(Alpha,Belta,Udc)
%#codege
a=0;
b=0;
c=0;
x=0;
y=0;
z=0;
A=0;
B=0;

Output=0;
a=Belta;
b=0.5*(sqrt(3)*Alpha-Belta);
c=-0.5*(sqrt(3)*Alpha+Belta);

A=Alpha;
B=Belta;

x=1.732*B/Udc;
y=(1.5*A+0.866*B)/Udc;
z=(0.866*B-1.5*A)/Udc;

if a>0
    a=1;
else
```

```
    a=0;
end
if b>0
    b=1;
else
    b=0;
end
if c>0
    c=1;
else
    c=0;
end
N=int16(a+2*b+4*c);
if(N==0)
    N=int16(1);
end
switch (N)
    case 1              %%%Area 2
        Output=2;
        T1=y;
        T2=z;
    case 2              %%%Area 6
        Output=6;
        T1=-x;
        T2=y;
    case 3              %%%Area 1
        Output=1;
        T1=-z;
        T2=x;
    case 4              %%%Area 4
        Output=4;
        T1=z;
        T2=-x;
    case 5
        Output=3;       %%%Area 3
        T1=x;
        T2=-y;
    case 6              %%%Area 5
        Output=5;
        T1=-y;
        T2=-z;
    otherwise
        Output=1;
        T1=z;
        T2=y;
end
Area=N;
if((T1+T2)>1)           %%% Over-modulation
    T1=T1/(T1+T2);
    T2=T2/(T1+T2);
end
```

E.5 Firing time calculation

```
function [Ta,Tb,Tc]= fcn(Sector,Time)
TA=0;
```

```
TB=0;
TC=0;
TD=0;
Ts=1e-4;
TA=Time(3)/4;
TB=Time(1)/2+TA;
TC=Time(2)/2+TA;
TD=Time(1)/2+Time(2)/2+TA;

switch (int16(Sector))
    case 1
        Ta=TB;
        Tb=TD;
        Tc=TA;
    case 2
        Ta=TD;
        Tb=TA;
        Tc=TB;
    case 3
        Ta=TD;
        Tb=TC;
        Tc=TA;
    case 4
        Ta=TA;
        Tb=TB;
        Tc=TD;
    case 5
        Ta=TA;
        Tb=TD;
        Tc=TC;
    case 6
        Ta=TC;
        Tb=TA;
        Tc=TD;
    otherwise
        Ta=Time(3)/4;
        Tb=Time(3)/4;
        Tc=Time(3)/4;
end
Ta=Ta*2;
Tb=Tb*2;
Tc=Tc*2;
```

Appendix F Central Control Program

F.1 Main function codes

```
/*=================================================*/
#include <LPC213X.H>
#include "initPLL.h"
#include "pwm.h"
#include "Timer.h"
#include "adc.h"
#include "definition.h"
/*=================================================*/
extern void ExtInit(void);
/*=================================================*/
int main(void)
{
        InitPLL();
        IO0DIR|=OPRLY;
        SETIO0(OPRLY,0);   //Switched off inverter output
        InitDAC();                          //Initialised DAC function
        InitADC();                          //Initialised ADC function
        ExtInit();
        InitTimer0();
        while(1);
        return 0;
}
/*=================================================*/
```

F.2 Configure PLL

```
/*=================================================*/
#define FOSC 11059200
//#define FOSC          10000000
```

```
#define FCCLK         FOSC*5
#define PCLK FCCLK/2
/*=================================================*/
void InitPLL(void)
{
        //The processor clock is configured 50MHz as the osciilator is 10MHz
        PLLCFG=(((FCCLK/FOSC)-1)|(2<<6));
        PLLCON=0x01;        //Enable pll and connect it
        PLLFEED=0xAA;       //Feeding pll
        PLLFEED=0x55;       //Fedding pll
        while(!(PLLSTAT&(1<<10)));
        PLLCON=0x03;
        PLLFEED=0xAA;       //Feeding pll
        PLLFEED=0x55;       //Fedding pll
        VPBDIV=0x02;        //The APB bus clock is half of the processor clock
}
/*=================================================*/
```

F.3 Timer 0 codes

```
/*=================================================*/
#define SAMPLE_POINT     256
#define FREQ_GRID 50
/*=================================================*/
void __irq Timer0_isr(void)
{
        static int Count=0;
        T0IR|=0x01;
        Count++;
        if(Count>=256)
        {
                Count=0;
        }
```

```
        if(Count==0)
        {
                SETIO0(OPRLY,0);
        }
        else if(Count==128)
        {
                SETIO0(OPRLY,1);
        }
        VICVectAddr=0;
}
/*=================================================*/
void InitTimer0(void)
{
        int mSecond5=0;
        VICIntSelect&=(~(1<<4));    // Assigning timer0 to irq interrupt
        VICVectCntl0=0x20|4;                // Slot 0 appoint to timer0 interrupt
        VICVectAddr0=(unsigned int)&Timer0_isr;
        VICIntEnable|=(1<<4);               // Enable the interrupt of timer0
        T0TCR=0;                            // Disable timer0 for configuration
        T0CTCR=0;                   // Timer model
        //The sampling frequency is configured as 50x256
        mSecond5=PCLK/FREQ_GRID/SAMPLE_POINT/10 - 1;
        T0PR=mSecond5;
        T0MCR=0x0003;                       // TC will be reset if MR0 matches it
        T0TCR=0x01;                 //Timer0 start to run
        T0MR0=9;
        VICVectAddr=0;                      //clear interrupt vector address
}
/*=================================================*/
```

Appendix G Inverter Program

G.1 Main function codes

```
/*================================================*/
#include <LPC213X.H>
#include "initPLL.h"
#include "pwm.h"
#include "Timer.h"
#include "adc.h"
#include "serial.h"
/*================================================*/
#defineS_OFF_GRID                    0
#define S_WAITING_ON_GRID_OUTPUT     1
#define S_ON_GRID_OUTPUT             2
#define S_WAITING_STOP_ON_GRID       3
#define S_WAITING_OFF_GRID_OUTPUT    4
#define S_OFF_GRID_OUTPUT            5
#define S_WAITING_STOP_OFF_GRID      6
#define OPRLY        (1<<25)
#define SETIO0(o,s)  { \
        if(s==0)                \
                IO0CLR|=o;      \
        else                    \
                IO0SET|=o;      \
}
#define SETIO1(o,s)  { \
        if(s==0)                \
                IO1CLR|=o;      \
        else                    \
                IO1SET|=o;      \
}
```

```
/*================================================*/
typedef struct{
        int16 State;
        int16 (*GetState)(void);
        void (*ChangeState)(int16);
}tagSystem;
typedef struct{
        uint32 Direction;
        uint32 (*GetDirection)(void);
        void (*ChangeDirection)(uint32);
}tagBridge;

extern unsigned int const Sinewave[SAMPLE_POINT];
extern void TestFunction(void);
extern void ExtInit(void);
int16 ReadSystemState(void );
void WriteSystemState(int16 Value);
uint32 KeyScan(void);
tagSystem System={S_OFF_GRID,ReadSystemState,WriteSystemState};
/*================================================*/
int16 ReadSystemState(void)
{
        return(System.State);
}
/*================================================*/
void WriteSystemState(int16 Value)
{
        System.State=Value;
}
/*================================================*/
void InitIO(void)
{
```

```
	IO1DIR=(1<<25);
	SETIO1(OPRLY,0);
#ifdef DEBUG
	IO1DIR=(1<<16);
	SETIO1(LINEZERO,1);
#endif
}
/*================================================*/
int main(void)
{
	int16 SystemState;
	InitPLL();
	PWMInitial();
	InitDAC();
	InitADC();
	InitUart1();
	ExtInit();
	InitIO();
	InitTimer0();
	while(1)
	{
		if(!KeyScan())
		{
			SystemState=System.GetState();
#ifdef DEBUG
			//The system is operating on grid
			if(SystemState==S_OFF_GRID)
			{
				//The system is Waiting to output to the grid
				System.ChangeState(S_WAITING_ON_GRID_OUTPUT);
			}
			else if(SystemState==S_ON_GRID_OUTPUT)
			//The system is outputing to the grid
```

```
                        {
                                //The system is waitting to off the grid
                                System.ChangeState(S_WAITING_STOP_ON_GRID);
                        }
#else
                        if(SystemState==S_OFF_GRID)
                        {
                                System.ChangeState(S_WAITING_OFF_GRID_OUTPUT);
                        }
                        else if(SystemState==S_OFF_GRID_OUTPUT)
                        {
                                System.ChangeState(S_WAITING_STOP_OFF_GRID);
                        }
#endif
                }
        }
        return 0;
}
/*================================================*/
#define SW_ON       (1<<10)
void DelaymS(uint16 mSecond)
{
        uint16 i;
        while(--mSecond)
        {
                i=10000;
                while(--i);
        }
}
/*================================================*/
uint32 KeyScan(void)
{
```

```
	uint32 KeyValue=0;
	KeyValue=IO0PIN;
	KeyValue&=SW_ON;
	if(KeyValue==0)
	{
		DelaymS(1);
		do{
			KeyValue=IO0PIN;
			KeyValue&=SW_ON;
		}while (KeyValue==0);
		KeyValue=0;
	}
	return KeyValue;
}
/*================================================*/
```

G.2 Extern interrupts codes

```
/*================================================*/
#include <LPC213X.H>
#include "pwm.h"
#include "main.h"
#include "definition.h"
//Timer0	VICVectCntl0
//Ext3		VICVectCntl3
//Ext2		VICVectCntl4
//Uart1		VICVectCntl5
extern tagBridge Bridge;
extern tagSystem System;
extern unsigned int PeroidReset;
extern unsigned int Count;
void __irq ExtINT3_isr(void);
void __irq ExtINT2_isr(void);
```

```
/*=================================================*/
void ExtInit(void)
{
	PINSEL0&=0x3FFFFFFF;
	PINSEL0|=0x80000000;		// P0.15 is asigned to EINT2
	PINSEL1&=0xCFFFFFFF;
	PINSEL1|=0x20000000;		// P0.30 is asigned to EINT3
	EXTMODE|=((1<<2)|(1<<3));	// Ext2 and Ext3 is edge sensetive
	EXTPOLAR|=((1<<2)|(1<<3));	// Ext2 and Ext3 is rising-edge sensitive
	VICIntSelect&=(~(1<<16));	// Assigning Ext2 to irq interrupt
	VICIntSelect&=(~(1<<17));	// Assigning Ext3 to irq interrupt
	VICVectCntl4=0x20|16;		// Slot 4 appoint to Ext3 interrupt
	VICVectCntl3=0x20|17;		// Slot 3 appoint to Ext3 interrupt
	VICVectAddr3=(unsigned int)&ExtINT3_isr;
	VICVectAddr4=(unsigned int)&ExtINT2_isr;
	VICIntEnable|=(1<<16);		// Enable the interrupt of ExtINT2
	VICIntEnable|=(1<<17);		// Enable the interrupt of ExtINT3
	EXTINT|=((1<<2)|(1<<3));	// Clear extenal interrupt 2 and3
}
/*=================================================*/
void __irq ExtINT3_isr(void)
{
	uint32 Direction=POSITIVE;
	uint32 SystemState;
	EXTINT|=(1<<3);				// Clear extenal interrupt 3
	SystemState=System.GetState();
	if(SystemState==S_WAITING_ON_GRID_OUTPUT)
	{
		SystemState=S_ON_GRID_OUTPUT;
		System.ChangeState(SystemState);
		SETIO1(OPRLY,1);
	}
```

```
        else if(SystemState==S_WAITING_STOP_ON_GRID)
        {
                SystemState=S_OFF_GRID;
                System.ChangeState(SystemState);
                SETIO1(OPRLY,0);
        }
        if(SystemState==S_ON_GRID_OUTPUT)
        {
                Direction=Bridge.GetDirection();
                Direction^=0x01;
                Bridge.ChangeDirection(Direction);
        }
        VICVectAddr=0;
}
/*================================================*/
void __irq ExtINT2_isr(void)
{
        EXTINT|=(1<<2);                         // Clear interrupt flag
        PeroidReset=1;
        VICVectAddr=0;                          // return interrupt routine
}
/*================================================*/
```

G.3 Timer 0 codes

```
/*================================================*/
#include <LPC213X.H>
#include "initPLL.h"
#include "Timer.h"
#include "PWM.h"
#include "adc.h"
#include "definition.h"
/*================================================*/
unsigned int SinePointer=0;
unsigned int SampleOrder=INC_DIR;
unsigned int Count=0;
unsigned int PeroidReset=0;
//unsigned int Direction=POSITIVE;
extern tagFIR FIR;
extern tagSystem System;
extern tagBridge Bridge;
/*================================================*/
unsigned int const Sinewave[HALF_SAMPLE_POINT]=
{
        0,25,49,74,98,122,147,171,195,219,243,267,290,314,337,360,
        383,405,428,450,471,493,514,535,556,576,596,615,634,653,672,690,
        707,724,741,757,773,788,803,818,831,845,858,870,882,893,904,914,
        924,933,942,950,957,964,970,976,981,985,989,992,995,997,999,1001,
        1001,1001,999,997,995,992,989,985,981,976,970,964,957,950,942,933,
        924,914,904,893,882,870,858,845,831,818,803,788,773,757,741,724,
        707,690,672,653,634,615,596,576,556,535,514,493,471,450,428,405,
        383,360,337,314,290,267,243,219,195,171,147,122,98,74,49,25
};
/*================================================*/
void __irq Timer0_isr(void)
```

```
{
        static int i=0;
        static int HistoryDir=POSITIVE;
        uint32 Direction;
        unsigned int Value;
        int16 SystemState;
        T0IR|=0x01;
        if(PeroidReset)
        {
                PeroidReset=0;
                Count=0;
        }
        Value=Sinewave[i];
        Value*=9;                                       //The output 90% of full
        Value/=10;
        i++;
        SystemState=System.GetState();
        Direction=Bridge.GetDirection();
        if(i>=HALF_SAMPLE_POINT)
        {
                i=0;
                //The system is going to output in off-grid mode
                if(SystemState==S_WAITING_OFF_GRID_OUTPUT)
                {
                        System.ChangeState(S_OFF_GRID_OUTPUT);
                        SystemState=S_OFF_GRID_OUTPUT;
                        SETIO1(OPRLY,1);
                }else if(SystemState==S_WAITING_STOP_OFF_GRID)
                //The system is going to stop output in off-grid mode
                {
                        System.ChangeState(S_OFF_GRID);
                        SystemState=S_OFF_GRID;
                        SETIO1(OPRLY,0);
```

```
        }
}
if(SystemState==S_OFF_GRID_OUTPUT)  //Off-grid output
{
        if(i==0)
        {
                Direction^=1;
                Bridge.ChangeDirection(Direction);
                ZeroCrossing(Direction);
        }
        if(Direction==POSITIVE)
        {
                PWMMR1=Value;
                PWMMR5=Value;
                PWMLER=((1<<1)|(1<<5));
        }
        else
        {
                PWMMR3=Value;
                PWMMR2=Value;
                PWMLER=((1<<2)|(1<<3));
        }
}
else if (SystemState==S_ON_GRID_OUTPUT)       //On-grid output
{
        Direction=Bridge.GetDirection();
        PWM_UpgradeValue(Value,Direction);
        if(Direction!=HistoryDir)
        {
                HistoryDir=Direction;
                ZeroCrossing(Direction);
        }
```

```
        }
        else
        {
                PWM2_IO_LOW();
                PWM5_IO_LOW();
                PWM1_IO_LOW();
                PWM3_IO_LOW();
                SETIO1(OPRLY,0);
        }
        VICVectAddr=0;
}
/*=================================================*/
void InitTimer0(void)
{
        int mSecond5=0;
        VICIntSelect&=(~(1<<4));            // Assigning timer0 to irq interrupt
        VICVectCntl0=0x20|4;                // Slot 0 appoint to timer0 interrupt
        VICVectAddr0=(unsigned int)&Timer0_isr;
        VICIntEnable|=(1<<4);               // Enable the interrupt of timer0
        T0TCR=0;                            // Disable timer0 for configuration
        T0CTCR=0;                           // Timer model
        mSecond5=PCLK/FREQ_GRID/SAMPLE_POINT/10 - 1;
        T0PR=mSecond5;
        T0MCR=0x0003;                       // TC will be reset if MR0 matches it
        T0TCR=0x01;
        T0MR0=9;
        VICVectAddr=0;
}
/*=================================================*/
```

G.4 PWM generator codes

```
/*================================================*/
#include <LPC213X.H>
//#include <LPC21xx.H>
#include "main.h"
#include "pwm.h"
#define PWM1_BITS 0
#define PWM2_BITS 14
#define PWM3_BITS 2
#define PWM5_BITS 10
typedef struct{
	uint32 Direction;
	uint32 (*GetDirection)(void);
	void (*ChangeDirection)(uint32);
}tagBridge;
tagBridge Bridge={POSITIVE,ReadDirection,WriteDirection};
void __irq isr_PWM(void);
/*================================================*/
void ZeroCrossing(unsigned int Direction)
{
	if (Direction==POSITIVE)
	{
		//First step is Disable PWM3 output
		PWM3_IO_LOW();
		PWM2_IO_LOW();
		PWM1Connect();
		PWM5Connect();
	}
	else
	{
		PWM1_IO_LOW();
```

```
                PWM5_IO_LOW();
                PWM3Connect();
                PWM2Connect();
        }
}
/*================================================*/
void PWMInitial(void)
{
        IO0DIR|=(0x00000003|(1<<PWM2_IO)|(1<<PWM5_IO));
        PINSEL0|=(2<<PWM1_BITS|2<<PWM2_BITS)|(2<<PWM3_BITS);
        PINSEL1|=(1<<PWM5_BITS);
        PWM1_IO_LOW();
        PWM3_IO_LOW();
        PWM2_IO_LOW();
        PWM5_IO_LOW();
        PWMPCR=((1<<PWM1ENA)|(1<<PWM3ENA)
                        |(1<<PWM2ENA)|(1<<PWM5ENA));
        PWMTCR=0x02;                            //reset pwm timer counter
        PWMPR=0;                                // no prescale
        PWMMCR=0x02;
        PWMMR0=1000;
        PWMLER=0x0B;
        PWMTCR=0x09;
}
/*================================================*/
uint32 ReadDirection(void)
{
        return Bridge.Direction;
}
/*================================================*/
void WriteDirection(uint32 Direction)
{
```

```
	Bridge.Direction=Direction;
}
/*================================================*/
void PWM_UpgradeValue(uint32 Value, uint32 Direction)
{
	if(Direction==POSITIVE)
	{
		PWMMR1=Value;
		PWMMR5=Value;
		PWMLER=((1<<1)|(1<<5));
	}
	else
	{
		PWMMR3=Value;
		PWMMR2=Value;
		PWMLER=((1<<2)|(1<<3));
	}
}
/*================================================*/
```

Appendix H Three-phase SVPWM Rectifier Program

H.1 Three-phase rectifier with PFC codes

```
/*================================================*/
#include "DSP28x_Project.h"
#include "definition.h"
#include <math.h>
/*================================================*/
#define RATE_MODULATION      1
#define OFFSET       500
#define MAX_VALUE_COMP       1000//1875
#define MAX_SAMPLE_VAL       4095
#define MAX_INPUT_VOL  3
#define GRID_FRE    50
#define LIN_VAL     2.5E-3
#define TS      1000

#define MAX_AC_CURRENT       50
#define MAX_DC_BUS           750
#define SAMPLE_GAIN      MAX_SAMPLE_VAL/MAX_INPUT_VOL

#define VOL_CROSS_ZERO       1706 //4095*1.25/3
#define CUR_CROSS_ZERO       2048
#define VOL_GAIN   300
#define CUR_GAIN   25
#define MODULATION_RATE      1

#define DC_BUS       600
//Sampling Frequency
```

```
//          12.8K
#define A1      -1.961
#define A2      0.96159
#define B0      0.01921
#define B1      -0.01921
#define B2      0.0002362
#define B3      2*B2
#define B4      B2
/*================================================*/
SOGIType PhaseAValue={0,0};
SOGIType PhaseBValue={0,0};
SOGIType PhaseCValue={0,0};
PLL PLLPhaseA={0,1};
extern void PWM_ModifyRate(TagModuleTime PWMTimer);
/*================================================*/
int GetAmplitude(ThreePhase *pInput)
{
        float Amplitude,Alpha,Beta;
        Alpha=2.0/3*pInput->PhaseA-
                2.0/3*0.5*(pInput->PhaseB+pInput->PhaseC);
        Beta=1.732/3*(pInput->PhaseB-pInput->PhaseC);
        Amplitude=Alpha*Alpha+Beta*Beta;
        Amplitude=sqrt(Amplitude);
        return((int)Amplitude);
}
/*================================================*/
float SOGIFilterA(float Value)
{
        float Temp1,Temp2,ReturnValue;
        Temp1=-1.961*PhaseAValue.Zeta1;
        Temp2=0.96159*PhaseAValue.Zeta2;
        Temp1=Temp1+Temp2;
```

```
	Temp1=Value-Temp1;
	Temp2=-0.01921*PhaseAValue.Zeta2;
	PhaseAValue.Zeta2=PhaseAValue.Zeta1;
	PhaseAValue.Zeta1=Temp1;
	Temp1=0.01921*Temp1;
	ReturnValue=Temp1+Temp2;
	return ReturnValue;
}
/*================================================*/
float SOGIFilterB(float Value)
{
	float Temp1,Temp2,ReturnValue;
	Temp1=-1.961*PhaseBValue.Zeta1;
	Temp2=0.96159*PhaseBValue.Zeta2;
	Temp1=Temp1+Temp2;
	Temp1=Value-Temp1;
	Temp2=-0.01921*PhaseBValue.Zeta2;
	PhaseBValue.Zeta2=PhaseBValue.Zeta1;
	PhaseBValue.Zeta1=Temp1;
	Temp1=0.01921*Temp1;
	ReturnValue=Temp1+Temp2;
	return ReturnValue;
}
/*================================================*/
float SOGIFilterC(float Value)
{
	float Temp1,Temp2,ReturnValue;
	Temp1=-1.961*PhaseCValue.Zeta1;
	Temp2=0.96159*PhaseCValue.Zeta2;
	Temp1=Temp1+Temp2;
	Temp1=Value-Temp1;
	Temp2=-0.01921*PhaseCValue.Zeta2;
```

```
	PhaseCValue.Zeta2=PhaseCValue.Zeta1;
	PhaseCValue.Zeta1=Temp1;
	Temp1=0.01921*Temp1;
	ReturnValue=Temp1+Temp2;
	return ReturnValue;
}
/*================================================*/
float SOGIFilter(SOGIType *pNode,float Value)
{
	float Temp1,Temp2,ReturnValue;
	Temp1=pNode->Zeta1*A1;
	Temp2=pNode->Zeta2*A2;
	Temp1=Temp1+Temp2;
	Temp1=Value-Temp1;
	Temp2=pNode->Zeta2*B1;
	pNode->Zeta2=pNode->Zeta1;
	pNode->Zeta1=Temp1;
	Temp1=Temp1*B0;
	ReturnValue=Temp1+Temp2;
	return ReturnValue;
}
/*================================================*/
void PLLFilter(SOGIType *pNode,PLL *pPLL, float Value)
{
	float Node0,Node1,Node2,Temp1,Temp2,Temp3;
	Node1=pNode->Zeta1;
	Node2=pNode->Zeta2;
	Temp1=pNode->Zeta1*A1;
	Temp2=pNode->Zeta2*A2;
	Temp1=Temp1+Temp2;
	Node0=Value-Temp1;
	Temp2=pNode->Zeta2*B1;
```

```
	Temp1=Node0*B0;
	pPLL->Sin=Temp1+Temp2;

	Temp1=Node0*B2;
	Temp2=Node1*B3;
	Temp3=Node2*B4;
	pPLL->Cos=-(Temp1+Temp2+Temp3);
	pNode->Zeta2=Node1;
	pNode->Zeta1=Node0;
}
/*================================================*/
void PreProcessSamples(VISamples *pSample)
{
	static int Count=0;
	(*pSample).Voltage.PhaseA-=VOL_CROSS_ZERO;
	(*pSample).Voltage.PhaseA*=VOL_GAIN;
	(*pSample).Voltage.PhaseB-=VOL_CROSS_ZERO;
	(*pSample).Voltage.PhaseB*=VOL_GAIN;
	(*pSample).Voltage.PhaseC-=VOL_CROSS_ZERO;
	(*pSample).Voltage.PhaseC*=VOL_GAIN;

	(*pSample).Current.PhaseA-=CUR_CROSS_ZERO;
	(*pSample).Current.PhaseA*=CUR_GAIN;
	(*pSample).Current.PhaseB-=CUR_CROSS_ZERO;
	(*pSample).Current.PhaseB*=CUR_GAIN;
	(*pSample).Current.PhaseC-=CUR_CROSS_ZERO;
	(*pSample).Current.PhaseC*=CUR_GAIN;

	(*pSample).Voltage.PhaseA/=SAMPLE_GAIN;
	(*pSample).Voltage.PhaseB/=SAMPLE_GAIN;
	(*pSample).Voltage.PhaseC/=SAMPLE_GAIN;
	(*pSample).Current.PhaseA/=SAMPLE_GAIN;
```

```
	(*pSample).Current.PhaseB/=SAMPLE_GAIN;
	(*pSample).Current.PhaseC/=SAMPLE_GAIN;

	(*pSample).dcbus*=MAX_DC_BUS;
	(*pSample).dcbus/=MAX_SAMPLE_VAL;

	CurrentA=SOGIFilter(&PhaseAValue,(*pSample).Current.PhaseA);
	CurrentB=SOGIFilter(&PhaseBValue,(*pSample).Current.PhaseB);
	CurrentC=SOGIFilter(&PhaseCValue,(*pSample).Current.PhaseC);
	(*pSample).Current.PhaseA=CurrentA;
	(*pSample).Current.PhaseB=CurrentB;
	(*pSample).Current.PhaseC=CurrentC;
	Temp=SOGIFilterA((*pSample).Voltage.PhaseA);
	(*pSample).Voltage.PhaseA=Temp;

	Temp=SOGIFilterB((*pSample).Voltage.PhaseB);
	(*pSample).Voltage.PhaseB=Temp;

	Temp=SOGIFilterC((*pSample).Voltage.PhaseC);
	(*pSample).Voltage.PhaseC=Temp;
}
/*================================================*/
void ClarkeTransf(ThreePhase *pInput, ClarkeType *pOutput)
{
	pOutput->Alpha=2.0/3*pInput->PhaseA-
				2.0/3*0.5*(pInput->PhaseB+pInput->PhaseC);
	pOutput->Beta=1.732/3*(pInput->PhaseB-pInput->PhaseC);
}
/*================================================*/
void InvParkTransf(InvParkType *Input, ClarkeType *Output)
{
	Output->Alpha=Input->Cos*Input->ParkOut.Direct-
```

```
                        Input->Sin*Input->ParkOut.Quadrature;
    Output->Beta=Input->Cos*Input->ParkOut.Quadrature+
                        Input->Sin*Input->ParkOut.Direct;
}
/*=============================================*/
void ParkTransf(ParkInputType *Input, ParkType *Output)
{
    Output->Direct=Input->Stationary.Alpha*Input->Cos+
                        Input->Stationary.Beta*Input->Sin;
    Output->Quadrature=Input->Stationary.Beta*Input->Cos-
                            Input->Stationary.Alpha*Input->Sin;
}
/*=============================================*/
void PhaseLockedLoop(ParkInputType *pVoltage,PLL *pll)
{
    float Amplitude=0;
    Amplitude=pVoltage->Stationary.Alpha*pVoltage->Stationary.Alpha+
                    pVoltage->Stationary.Beta*pVoltage->Stationary.Beta;
    Amplitude=sqrt(Amplitude);
    if(Amplitude>180)
    {
        pll->Cos=pVoltage->Stationary.Alpha/Amplitude;
        pll->Sin=pVoltage->Stationary.Beta/Amplitude;
    }
}
/*=============================================*/
void GetInvParkVal(InvParkType *pInvPark)
{
    float Vd,Vq,IDref,IQref;
    PIDController(pInvPark->DCVol,DC_BUS,&DCVoltage);
    IDref=DC_BUS-pInvPark->DCVol;
    IDref-=pInvPark->Current.Direct;
```

```
        PIDController(pInvPark->Current.Direct,DCVoltage.OuputValue,
                        &DirectCurrent);
        IQref=0-pInvPark->Current.Quadrature;
        PIDController(pInvPark->Current.Quadrature,0,&QuadratureCurrent);
        Vd=pInvPark->Current.Quadrature*(6.283185*GRID_FRE*LIN_VAL);
        Vd+=pInvPark->Voltage.Direct;
        Vd-=DirectCurrent.OuputValue;
        Vd-=IDref;

        Vq=pInvPark->Voltage.Quadrature;
        Vq-=QuadratureCurrent.OuputValue;
        Vq-=IQref;
        Vq-=pInvPark->Current.Direct*(6.283185*GRID_FRE*LIN_VAL);
        pInvPark->ParkOut.Direct=Vd;
        pInvPark->ParkOut.Quadrature=Vq;
}
/*================================================*/
void GetModuleTime(ClarkeType *pPointer, TagModuleTime *pCOMP)
{
        float a,b,c;
        unsigned int Area=0;
        float T1,T2,T0,X,Y,Z,TA,TB,TC,TD,TimerA,TimerB,TimerC;
        /*The variable a,b,c are used to determine sectors*/
        a=pPointer->Beta;
        b=0.866*pPointer->Alpha-0.5*pPointer->Beta;
        c=-0.866*pPointer->Alpha-0.5*pPointer->Beta;
        /*X,Y,Z are utilised to obtain module time*/
        X=(1.732*pPointer->Beta)*RATE_MODULATION/DC_BUS;
        Y=(1.5*pPointer->Alpha+0.866*pPointer->Beta)*
            RATE_MODULATION/DC_BUS;
        Z=(0.866*pPointer->Beta-1.5*pPointer->Alpha)*
            RATE_MODULATION/DC_BUS;
```

```
if(a>0)
        Area=1;
if(b>0)
        Area+=2;
if(c>0)
        Area+=4;
switch(Area)
{
        case 1:
                T1=Y;
                T2=Z;
                if((T1+T2)>1)
                {
                        T1=T1/(T1+T2);
                        T2=T2/(T1+T2);
                }
                T0=TS*(1-T1-T2);
                T1=TS*T1;
                T2=TS*T2;
                TA=T0/4;
                TB=T1/2+TA;
                TC=T2/2+TA;
                TD=T1/2+T2/2+TA;
                TimerA=TB;
                TimerB=TD;
                TimerC=TA;
                break;
        case 2:
                T1=-X;
                T2=Y;
                if((T1+T2)>1)
                {
```

```
            T1=T1/(T1+T2);
            T2=T2/(T1+T2);
        }
        T0=TS*(1-T1-T2);
        T1=TS*T1;
        T2=TS*T2;
        TA=T0/4;
        TB=T1/2+TA;
        TC=T2/2+TA;
        TD=T1/2+T2/2+TA;
        TimerA=TD;
        TimerB=TA;
        TimerC=TB;
        break;
case 3:
        T1=-Z;
        T2=X;
        if((T1+T2)>1)
        {
            T1=T1/(T1+T2);
            T2=T2/(T1+T2);
        }
        T0=TS*(1-T1-T2);
        T1=TS*T1;
        T2=TS*T2;
        TA=T0/4;
        TB=T1/2+TA;
        TC=T2/2+TA;
        TD=T1/2+T2/2+TA;
        TimerA=TD;
        TimerB=TC;
        TimerC=TA;
```

```
        break;
case 4:
        T1=Z;
        T2=-X;
        if((T1+T2)>1)
        {
                T1=T1/(T1+T2);
                T2=T2/(T1+T2);
        }
        T0=TS*(1-T1-T2);
        T1=TS*T1;
        T2=TS*T2;
        TA=T0/4;
        TB=T1/2+TA;
        TC=T2/2+TA;
        TD=T1/2+T2/2+TA;
        TimerA=TA;
        TimerB=TB;
        TimerC=TD;
        break;
case 5:
        T1=X;
        T2=-Y;
        if((T1+T2)>1)
        {
                T1=T1/(T1+T2);
                T2=T2/(T1+T2);
        }
        T0=TS*(1-T1-T2);
        T1=TS*T1;
        T2=TS*T2;
        TA=T0/4;
```

```
                TB=T1/2+TA;
                TC=T2/2+TA;
                TD=T1/2+T2/2+TA;
                TimerA=TA;
                TimerB=TD;
                TimerC=TC;
                break;
        case 6:
                T1=-Y;
                T2=-Z;
                if((T1+T2)>1)
                {
                        T1=T1/(T1+T2);
                        T2=T2/(T1+T2);
                }
                T0=TS*(1-T1-T2);
                T1=TS*T1;
                T2=TS*T2;
                TA=T0/4;
                TB=T1/2+TA;
                TC=T2/2+TA;
                TD=T1/2+T2/2+TA;
                TimerA=TC;  //Notice variable TC, TA and TD are float types
                TimerB=TA;
                TimerC=TD;
                break;
        }
        pCOMP->CompareA=(unsigned int)(TimerA+0.5);
        pCOMP->CompareB=(unsigned int)(TimerB+0.5);
        pCOMP->CompareC=(unsigned int)(TimerC+0.5);
}
/*============================================*/
```

```
void GeneratePWM(VISamples *pSample)
{
	float MaxValue,MinValue,PhaseA,PhaseB,PhaseC,Temp;
	static int i=0;
	static int ACAmplitude=0;
	static int PhaseLocked=0;
	static float PastSinValue=0.0001;
	ParkInputType Voltages;
	ParkInputType Currents;
	ParkType VParkOut;
	ParkType IParkOut;
	InvParkType InvParkInput;
	ClarkeType InvClarke;
	TagModuleTime Comp;

	TagModuleTime PWMTimer;
	PhaseA=0;
	PhaseB=0;
	PhaseC=0;
	PreProcessSamples(pSample);
	ACAmplitude=GetAmplitude(&((*pSample).Voltage));
	if(ACAmplitude>10)
	{
		if(i<1000)
			i++;
	}
	else
	{
		i=0;
		PWMTimer.CompareA=0;
		PWMTimer.CompareB=0;
		PWMTimer.CompareC=0;
```

```
        PWM_ModifyRate(PWMTimer);
}
if(i>=1000)
{
        PhaseA=(*pSample).Voltage.PhaseA;
        PhaseB=(*pSample).Voltage.PhaseB;
        PhaseC=(*pSample).Voltage.PhaseC;
        PhaseA/=ACAmplitude;
        PhaseB/=ACAmplitude;
        PhaseC/=ACAmplitude;

        ClarkeTransf(&(pSample->Current),&(Currents.Stationary));
        ClarkeTransf(&(pSample->Voltage),&(Voltages.Stationary));

        PhaseLockedLoop(&Voltages,&PLLPhaseA);
        if(PhaseLocked==1)
        {
                Voltages.Cos=PLLPhaseA.Cos;
                Voltages.Sin=PLLPhaseA.Sin;
                Currents.Cos=PLLPhaseA.Cos;
                Currents.Sin=PLLPhaseA.Sin;
                InvParkInput.Cos=PLLPhaseA.Cos;
                InvParkInput.Sin=PLLPhaseA.Sin;
                ParkTransf(&Voltages,&VParkOut);
                ParkTransf(&Currents,&IParkOut);
                InvParkInput.Voltage.Direct=VParkOut.Direct;
                InvParkInput.Voltage.Quadrature=VParkOut.Quadrature;
                InvParkInput.Current.Direct=IParkOut.Direct;
                InvParkInput.Current.Quadrature=IParkOut.Quadrature;
                InvParkInput.DCVol=pSample->dcbus;
                GetInvParkVal(&InvParkInput);
                InvParkTransf(&InvParkInput,&InvClarke);
```

```
                GetModuleTime(&InvClarke,&Comp);
        }
        else
        {
                if((PLLPhaseA.Sin>0)&&(PastSinValue<0))
                {
                        PhaseLocked=1;
                }
                else
                        PastSinValue=PLLPhaseA.Sin;
        }

    }
}
/*================================================*/
```

H.2 SVPWM generation

```
/*==================================================*/
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File
#include "definition.h"
//#define MAX_LEN  50
#define MAX_LEN    33
#define GOING_UP   1
#define GOING_DOWN       0
#define SYSCLK       150000000
#define EPWM_DIV  4
#define FR_SWITCH10K      1000//SYSCLK/2/EPWM_DIV/10000
/*==================================================*/
void InitPWM(void)
{
        EALLOW;
        GpioCtrlRegs.GPAMUX1.bit.GPIO0=1;
        GpioCtrlRegs.GPAMUX1.bit.GPIO1=1;
        GpioCtrlRegs.GPAMUX1.bit.GPIO2=1;
        GpioCtrlRegs.GPAMUX1.bit.GPIO3=1;
        GpioCtrlRegs.GPAMUX1.bit.GPIO4=1;
        GpioCtrlRegs.GPAMUX1.bit.GPIO5=1;
        GpioCtrlRegs.GPADIR.bit.GPIO0=1;
        GpioCtrlRegs.GPADIR.bit.GPIO1=1;
        GpioCtrlRegs.GPADIR.bit.GPIO2=1;
        GpioCtrlRegs.GPADIR.bit.GPIO3=1;
        GpioCtrlRegs.GPADIR.bit.GPIO4=1;
        GpioCtrlRegs.GPADIR.bit.GPIO5=1;

        EPwm1Regs.TBPRD=FR_SWITCH10K;
        EPwm1Regs.TBPHS.half.TBPHS=0;
        EPwm1Regs.TBCTL.bit.CTRMODE=TB_COUNT_UPDOWN;
```

```
EPwm1Regs.TBCTL.bit.PHSEN=TB_DISABLE;
EPwm1Regs.TBCTL.bit.PRDLD=TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL=TB_CTR_ZERO;
EPwm1Regs.TBCTL.bit.HSPCLKDIV=TB_DIV4;
EPwm1Regs.CMPCTL.bit.SHDWAMODE=CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE=CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE=CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.LOADBMODE=CC_CTR_ZERO;

EPwm1Regs.AQCTLA.bit.CAU=AQ_CLEAR;
EPwm1Regs.AQCTLA.bit.CAD=AQ_SET;

EPwm1Regs.DBCTL.bit.OUT_MODE=DB_FULL_ENABLE;
EPwm1Regs.DBCTL.bit.POLSEL=DB_ACTV_HIC;
EPwm1Regs.DBFED=50;
EPwm1Regs.DBRED=50;

EPwm2Regs.TBPRD=FR_SWITCH10K;
EPwm2Regs.TBPHS.half.TBPHS=0;
EPwm2Regs.TBCTL.bit.CTRMODE=TB_COUNT_UPDOWN;
EPwm2Regs.TBCTL.bit.PHSEN=TB_ENABLE;
EPwm2Regs.TBCTL.bit.PRDLD=TB_SHADOW;
EPwm2Regs.TBCTL.bit.SYNCOSEL=TB_SYNC_IN;
EPwm2Regs.TBCTL.bit.HSPCLKDIV=TB_DIV4;
EPwm2Regs.CMPCTL.bit.SHDWAMODE=CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE=CC_SHADOW;
EPwm2Regs.CMPCTL.bit.LOADAMODE=CC_CTR_ZERO;
EPwm2Regs.CMPCTL.bit.LOADBMODE=CC_CTR_ZERO;

EPwm2Regs.AQCTLA.bit.CAU=AQ_CLEAR;
EPwm2Regs.AQCTLA.bit.CAD=AQ_SET;
```

```
    EPwm2Regs.DBCTL.bit.OUT_MODE=DB_FULL_ENABLE;
    EPwm2Regs.DBCTL.bit.POLSEL=DB_ACTV_HIC;
    EPwm2Regs.DBFED=50;
    EPwm2Regs.DBRED=50;

    EPwm3Regs.TBPRD=FR_SWITCH10K;
    EPwm3Regs.TBPHS.half.TBPHS=0;
    EPwm3Regs.TBCTL.bit.PHSEN=TB_ENABLE;
    EPwm3Regs.TBCTL.bit.CTRMODE=TB_COUNT_UPDOWN;
    EPwm3Regs.TBCTL.bit.PRDLD=TB_SHADOW;
    EPwm3Regs.TBCTL.bit.SYNCOSEL=TB_SYNC_IN;
    EPwm3Regs.TBCTL.bit.HSPCLKDIV=TB_DIV4;
    EPwm3Regs.CMPCTL.bit.SHDWAMODE=CC_SHADOW;
    EPwm3Regs.CMPCTL.bit.SHDWBMODE=CC_SHADOW;
    EPwm3Regs.CMPCTL.bit.LOADAMODE=CC_CTR_ZERO;
    EPwm3Regs.CMPCTL.bit.LOADBMODE=CC_CTR_ZERO;
    EPwm3Regs.AQCTLA.bit.CAU=AQ_CLEAR;
    EPwm3Regs.AQCTLA.bit.CAD=AQ_SET;

    EPwm3Regs.DBCTL.bit.OUT_MODE=DB_FULL_ENABLE;
    EPwm3Regs.DBCTL.bit.POLSEL=DB_ACTV_HIC;
    EPwm3Regs.DBFED=50;
    EPwm3Regs.DBRED=50;
    EPwm1Regs.TBCTR=0;
    EPwm2Regs.TBCTR=0;
    EPwm3Regs.TBCTR=0;
    EDIS;
}
/*=============================================*/
void PWM_ModifyRate(TagModuleTime PWMTimer)
{
    EPwm1Regs.CMPA.half.CMPA=PWMTimer.CompareA;
```

```
        EPwm2Regs.CMPA.half.CMPA=PWMTimer.CompareB;
        EPwm3Regs.CMPA.half.CMPA=PWMTimer.CompareC;
}
/*================================================*/
```

H.3 ADC sampling codes

```
/*================================================*/
#include "DSP28x_Project.h"
#include "definition.h"
#include <math.h>
/*================================================*/
#if(CPU_FRQ_150MHZ)
        #define ADC_MODCLK      0x03    // High speed peripherial clock
        // HSPCLK=SYSCLKOUT/(2*ADC_MODCLK)
#endif                          //HSPCLK=150M/(2*3)=25M

#if(CPU_FRQ_100MHZ)
        #define ADC_MODCLK      0x02
#endif

#define ADC_CKPS  0x3           //12.5MHz
#define ADC_SHCLK               0xf
#define SYSCLK              150000000
#define TS_1M         SYSCLK/2/1000000
#define TS_100K       SYSCLK/2/100000
#define TS_50K        SYSCLK/2/50000
#define TS_20K        SYSCLK/2/20000
#define TS_12_8K      SYSCLK/2/12800
#define TS_10K        SYSCLK/2/10000
#define TS_3K2        SYSCLK/2/3200
/*================================================*/
//#define ADC_Cal (void (*)(void))0x380080
extern void GeneratePWM(VISamples *);
Uint32 ConversionCount=0;
Uint16 Voltage1;
Uint16 Voltage2;
```

```
Uint16 Voltage3;
Uint16 Voltage4;
Uint16 Voltage5;
Uint16 Voltage6;
Uint16 Voltage7;
Uint16 Voltage8;
VISamples ADCSample;
TagModuleTime PWMTimer;
/*================================================*/
void ConfigureAdc(void)
{
        // Configure ADC
        EALLOW;
        AdcRegs.ADCTRL1.bit.SEQ_CASC=1;
        AdcRegs.ADCTRL3.bit.SMODE_SEL=0;
        AdcRegs.ADCTRL3.bit.ADCCLKPS=ADC_CKPS;
        AdcRegs.ADCTRL1.bit.ACQ_PS=ADC_SHCLK;
        AdcRegs.ADCMAXCONV.all = 0x0007;       // Setup 2 conv's on SEQ1
        // Setup ADCINA3 as 1st SEQ1 conv.
        AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0;
        // Setup ADCINA2 as 2nd SEQ1 conv.
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1;
        AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x2;
        AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x3;
        AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 0x4;
        AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 0x5;
        AdcRegs.ADCCHSELSEQ2.bit.CONV06 = 0x6;
        AdcRegs.ADCCHSELSEQ2.bit.CONV07 = 0x7;
        AdcRegs.ADCOFFTRIM.all=0x01FA;        //Offset value is -6
        // Enable SOCA from ePWM to start SEQ1
        AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1;
        // Enable SEQ1 interrupt (every EOS)
```

```
        AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1=1;
        AdcRegs.ADCTRL1.bit.CONT_RUN=1;
        EPwm4Regs.ETSEL.bit.SOCAEN = 1;        // Enable SOC on A group
        // Select SOC from from CPMA on upcount
        EPwm4Regs.ETSEL.bit.SOCASEL=4;
        EPwm4Regs.ETPS.bit.SOCAPRD = 1;        // Generate pulse on 1st event
        EPwm4Regs.CMPA.half.CMPA = 0x0080;    // Set compare A value
        EPwm4Regs.TBPRD = TS_12_8K;             // Set period for ePWM1
        EPwm4Regs.TBCTL.bit.CTRMODE = 0;                // count up and start
        EDIS;
}
/*=============================================*/
interrupt void  adc_isr(void)
{
        Voltage1 = (AdcRegs.ADCRESULT0 >>4); //AN0
        Voltage2 = (AdcRegs.ADCRESULT1 >>4);
        Voltage3 = (AdcRegs.ADCRESULT2 >>4);
        Voltage4 = (AdcRegs.ADCRESULT3 >>4);
        Voltage5 = (AdcRegs.ADCRESULT4 >>4);
        Voltage6 = (AdcRegs.ADCRESULT5 >>4);
        Voltage7 = (AdcRegs.ADCRESULT6 >>4);
        Voltage8 = (AdcRegs.ADCRESULT7 >>4);
        ADCSample.Voltage.PhaseA=Voltage5;
        ADCSample.Current.PhaseA=Voltage6;
        ADCSample.Voltage.PhaseB=Voltage3;
        ADCSample.Current.PhaseB=Voltage4;
        ADCSample.Voltage.PhaseC=Voltage1;
        ADCSample.Current.PhaseC=Voltage2;
        ADCSample.dcbus=Voltage7;
        GeneratePWM(&ADCSample);
        Voltage1=0;
        Voltage2=0;
```

```
        Voltage3=0;
        Voltage4=0;
        Voltage5=0;
        Voltage6=0;
        Voltage7=0;
        Voltage8=0;
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
        AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1 bit
        // Acknowledge interrupt to PIE
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
        return;
}
/*===========================================*/
```

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